

# WBS 1.08.03 L3: Observatory DAQ Bolometer Readout Interfaces

#### L3 Lead - Nathan Whitehorn



WBS 1.08 DAQ Conceptual Design Review - July 24, 2023

#### Outline

- Presenter Introduction
- Key L3 contributors
- Breakdown of this L3
- Key Requirements
- Interfaces with other L3s
- Technical Design / Scope
- Prototyping Plans
- Conclusion



#### **Presenter Introduction**

Name: Nathan Whitehorn

Institution: Michigan State University

**Discipline:** Physics / Astrophysics

Previous experience: Development of SPT-3G DAQ software framework, current DAQ lead (hardware/software) for Pacific Ocean Neutrino Experiment, extensive experience with analysis and detectors for IceCube and SPT.



### **Key Contributors in this L3**

Nathan Whitehorn (MSU)

Christopher Weaver (Michigan State)

Sasha Rahlin (Chicago)



### **Description of L4 WBSs for your L3**

Lvl 2	Lvl 3	Lvl 4
1.08 Observatory Control and Data Acquisition Systems	1.08.01 - DAQ Management	1.08.01.01 - DAQ Management
		1.08.01.02 - DAQ System Design Engineering
		1.08.01.03 - DAQ Reviews
		1.08.01.04 - Interface Documentation
		1.08.01.05 - Specification Tracking
		1.08.01.06 - DAQ Milestones
	1.08.01 - Observatory Control System	1.08.02.01 - Bolometer Readout Control
		1.08.02.02 - Telescope Platform Control - SP, Chile, LAT, SAT
		1.08.02.03 - Cryogenic Control
		1.08.02.04 - Housekeeping Control
		1.08.02.05 - Observatory Subsystem Control
		1.08.02.06 - Build/Distribution System (Control System )
		1.08.02.07 - Scheduling
		1.08.02.08 - Control Framework
	1.08.03 - Observatory Data Acquisition	1.08.03.01 - Bolometer Readout
	1.08.03 - Observatory Data Acquisition	1.08.03.01 - Bolometer Readout 1.08.03.02 - Telescope Readout Data Acquisition
	1.08.03 - Observatory Data Acquisition	1.08.03.01 - Bolometer Readout 1.08.03.02 - Telescope Readout Data Acquisition 1.08.03.03 - Housekeeping Data Acquisition
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### Key Driving Requirements for DAQ Detector Readout Interface



Data for detectors: 83 Mbps (per SAT) 1.7 Gbps (LAT)

- Acquire detector data from readout boards at speeds of up to 10 Gbit/s (500k detectors, 32-bit sample, 400 Hz rate) and associated meta-data.
- Acquire time-stamped data from auxiliary sensors (cryostat thermometers, pressure sensors, flow sensors, motor currents, etc.) with time stamps accurate to well less than the detector sampling interval (~ 1 ms).
- Acquire asynchronous data at a variety of cadences (up to ~100 Hz)
- Read out telescope position axes (azimuth, elevation, boresight, and perhaps other fast telescope housekeeping data) at rates up to ~200Hz



#### Inter-L3 Interfaces within this L2



 Bolometer Readout (1.08.03.01) is a part of DAQ (1.08.03) and will interact with OCS (1.08.02), Lab support (1.08.05), and Integration, deployment (1.08.06)

#### **Technical Design / Scope**

CQ2

Acquire and aggregate high-speed data from detectors (400 Hz per detector, ~ 10 Gbit/s total) and hand off to data management



#### Moving from Stage-3 to Stage-4: Detector Readout DAQ

#### Problem scope:

• Data rate increasing from ~20k detectors per site to 300k: order-of-magnitude in data rate

#### Reusability:

- Order-of-magnitude increase in data rate and new readout electronics mean Stage-3 code is probably not useful.
- Architecture is scalable however; synthetic testing of order-of-magnitude higher sampling rates on SPT-3G readout meet S4 throughput requirements

#### Summary:

- Stage-3 DAQ systems **demonstrate required throughput**, can serve as an architectural and resource-use guide for S4
- Limited applicability of stage-3 DAQ code and hardware for detector readout
- Substantial development effort required, but little risk of unknown problems

### **Technical Design / Scope**



What is the state of development of the design?

- Readout/DAQ Interfaces have been defined in ICD
- Data cable from readout will be 10 Gbit Ethernet
- Designed from existing approaches in SPT-3G, SO
- Software architecture for interface computer has been demonstrated
- Initial emulators developed and software testbed in the lab connects to them and meets throughput requirements
  - Uses UDP transport with retransmit architecture designed for largely-reliable networks
  - Validated at 2x the data rate for an S4 LAT
  - Inputs and outputs similar to, or the same as, draft interfaces

## **Prototyping Plans**

- Prototype readout boards and software architecture have been demonstrated
- Intention is to evolve current system towards a lab-deployable framework:
  - Currently have in-house DAQ-developed board emulator that meets throughput requirements but does not implement the final readout/DAQ interface.
  - Readout L2 plans to provide a more realistic emulator for use by DAQ in ~ fall. C. Weaver traveling to SLAC in August to discuss interfaces. DAQ interface will be adapted to use that.
  - DAQ software will then be tested against prototype
- Once working with prototype electronics in the lab, system will evolve into final observatory DAQ

#### Conclusions

The team has experience with readout/DAQ from Stage-3 experiments and an early testing platform in place that meets requirements in synthetic tests.

DAQ will interact with OCS, Integration and Testing, and Lab Support L3's

DAQ will interact with Readout L2

Next steps will be to define and implement the interface to readout electronics in full detail.



#### **Backup Slides**



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