Readout Status

Zeeshan Ahmed (he/him)

CMB-S4 Collaboration Meeting
April 3-6, 2023

Outline

- Subsystem Team
- Scope
- Changes due to AoA
- Technical progress over last year
- Near-term plans
- Summary

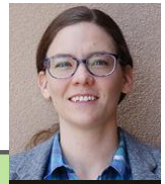
Team Has ~30 Scientists And Engineers With Expertise In Superconducting Sensor Readout And Low-Noise Electronics

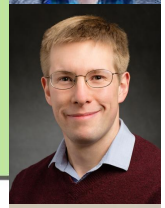
Readout Working Group
(CMB-S4 Collaboration)

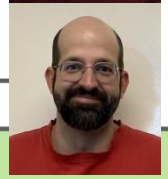
1.04
READOUT

Zeesh Ahmed
(SLAC)
Gunther Haller
(SLAC)

Readout Scientists
Darcy Barron (UNM)
Jeffrey Filippini (UIUC)
Shawn Henderson (SLAC)







1.04.01
Readout Management
Gunther Haller (SLAC)

1.04.02
Cryo 100mK Electronics
Leonid Sapozhnikov (SLAC)

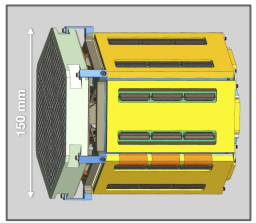
1.04.03
Cold 4K Electronics
Leonid Sapozhnikov (SLAC)

1.04.04
Warm Electronics
Ben Reese (SLAC)

1.04.05
Readout String Test
Shawn Henderson (SLAC)

Readout Working Group meets biweekly Thursdays 1p Pacific/3p Central

Readout Subsystem: Provide Superconducting And Traditional Electronics Systems To Bias TESs, Measure Current, And Amplify Signals, Using Time-Division Multiplexing (TDM)



Contains SQUID Series Array Amplifier

Cryogenic cabling

Start with MCE crates, upgrade with new warm modules.

100mK stage

4K stage

300K stage

Light from telescope

Detector and readout module

1-6x

feedhorn

photonic choke

waveguide interface plate

detector wafer

backshort

100mK readout module

superconducting flex

25-wire NbTi cable

100-wire manganin cable

4K SSA module

4K SSA module

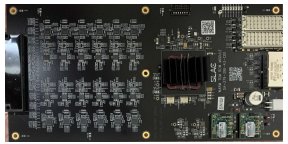
4K SSA module

300K readout module

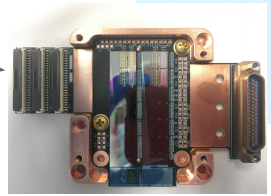
300K readout module

300K readout module

Warm electronics modules



SQUID multiplexer and TES bias chips



100mK row address module

51-wire NbTi cable

4K row address module

51-wire manganin cable

300K row address module

CMB-S4

AoA Changes Are Being Incorporated Into Planning

No technical/design changes. Only production quantities of components have changed.

Component	Before AoA	After AoA
Detector-Readout Flex Cable (one per column)	4,619	4,214
100mK 2-level Mux Chips	88,600	74,806
100mK Readout Modules	2,432	2,053
4K SSA Module	1,174	985
300K Row Address Modules	496	383
300K Column Readout Modules	1,174	985

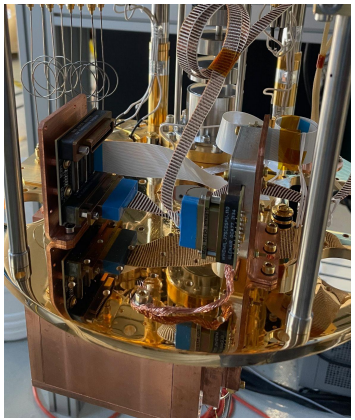
Numbers include yield/production losses. Refer to J. Ruhl/pBD for official counts

Detector And Readout Teststands Are Coming Online

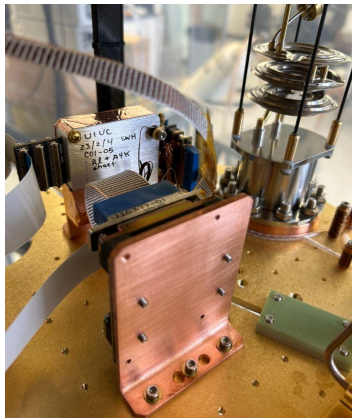
Detector test stands at **FNAL, SLAC and UIUC** now operational with cryogenic and warm readout components.

Bringing an additional readout characterization and testing setup online at **UNM** for cryogenic component characterization (cable bandwidths, thermal properties etc.)

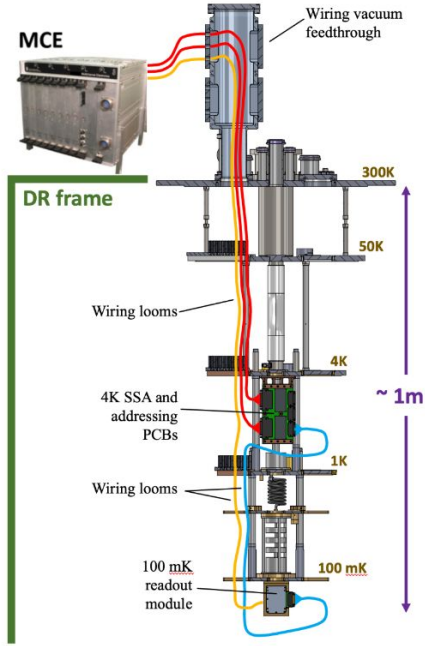
UNM Readout characterization



100 mK Readout in FNAL cryostat



100 mK Readout in UIUC cryostat



Typical CMB-S4 teststand (SLAC pictured)

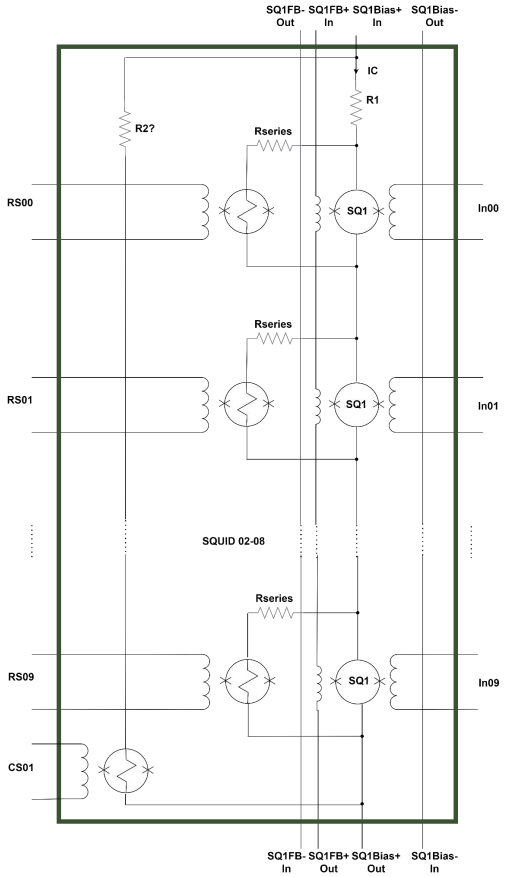
2-Level Superconducting 100 mK Multiplexer Chip and 4K SSA Designed, To Be Fabricated by NIST

To reduce wiring, upgrading from *single-level addressing (80 row addresses)* to *two-level addressing (10 row addresses plus 8 chip selects)*

- 80-pair cable → 18-pair cable from 300K to 100mK
- Enables connections from top of Si wiring chip holding superconducting chips

MUX chips were designed and prototypes were ordered from NIST, in fabrication queue.

A “faster” 4K Series SQUID Array also designed and being prototyped.

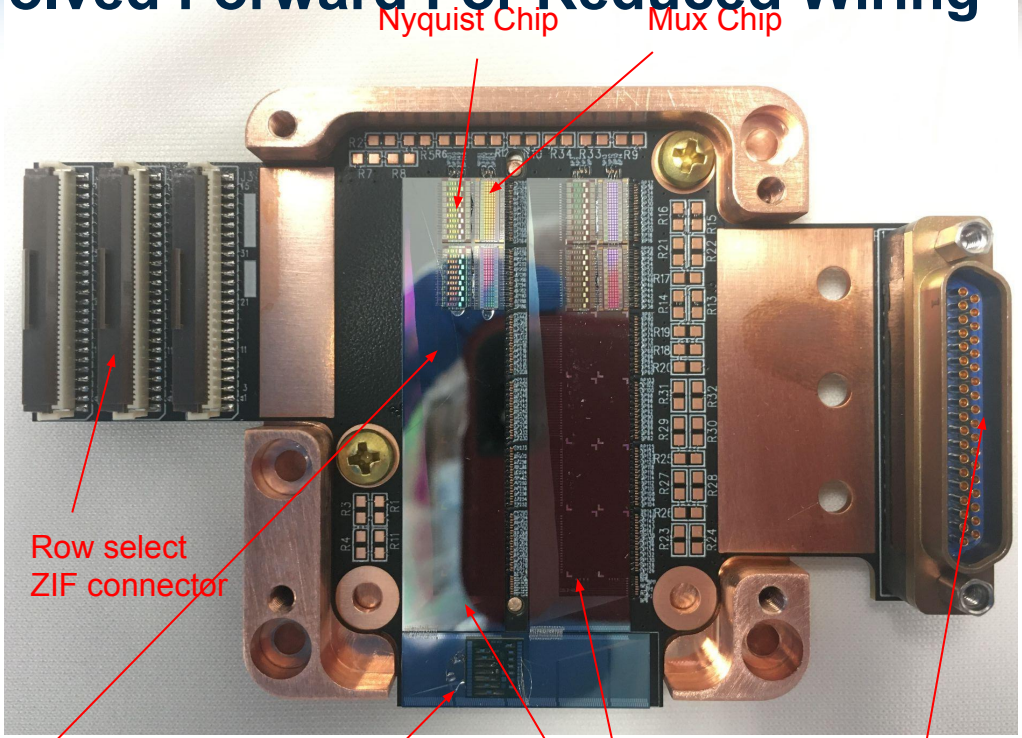


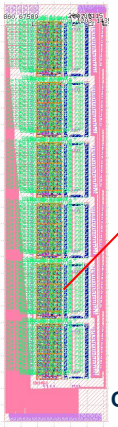
100 mK Readout Module Evolved Forward For Reduced Wiring And Improved Durability

Improved assembly processes from previous round including gluing, wirebonding, and handling.

Updating circuit boards and wiring chips support new 2-level MUX chips for *prototyping* while reusing most of the hardware, and reducing wire counts

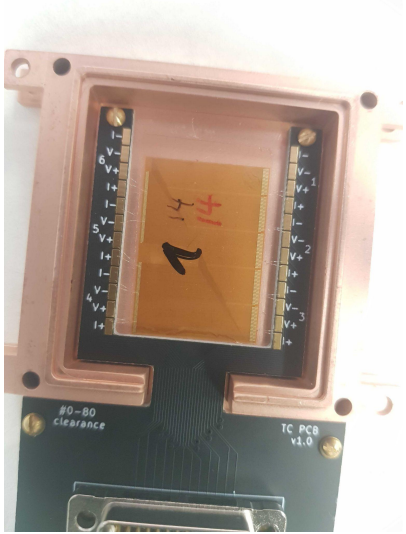
Continuing to record lessons for *production* modules



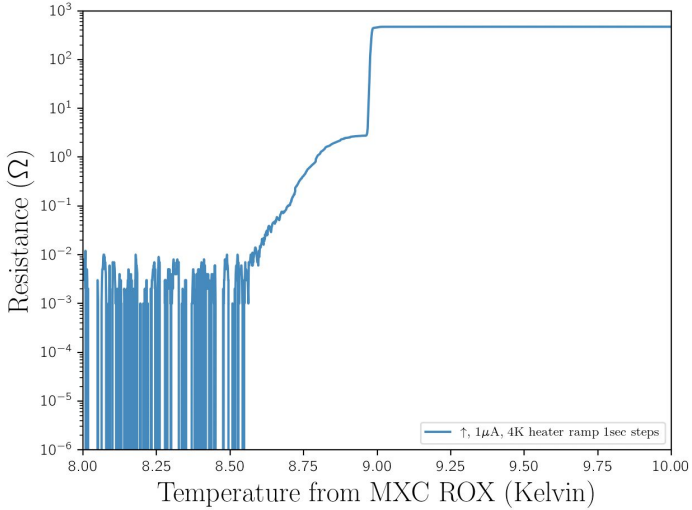


New Si adapter chip (designed but not fabricated yet)

Superconducting Flex Cables Are Being Developed at Hightec And CEA/France

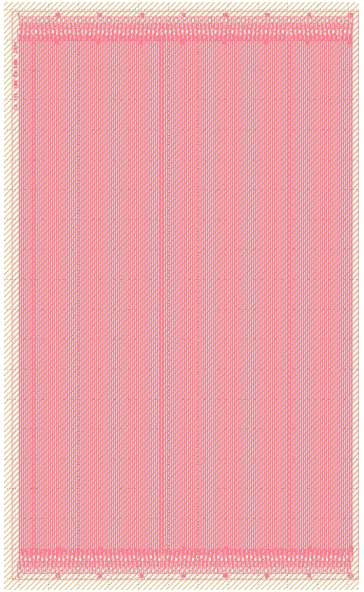


Flex prototype from Hightec in characterization setup. Wirebonded by FNAL. Low yield because of over-etching (will be addressed in next run)



Performance:
Superconducting ~ O(10) μOhm residual resistance at 4K, but critical current low in this run.

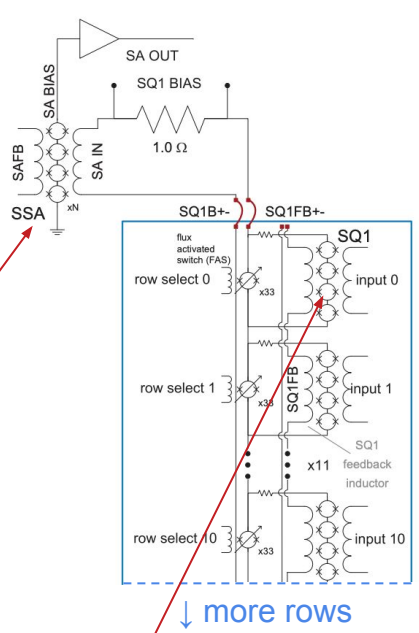
80 Nb trace pairs at 140 um pair pitch (70 um trace pitch)

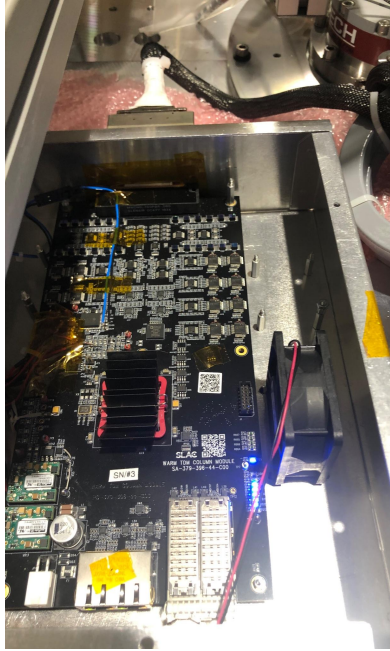


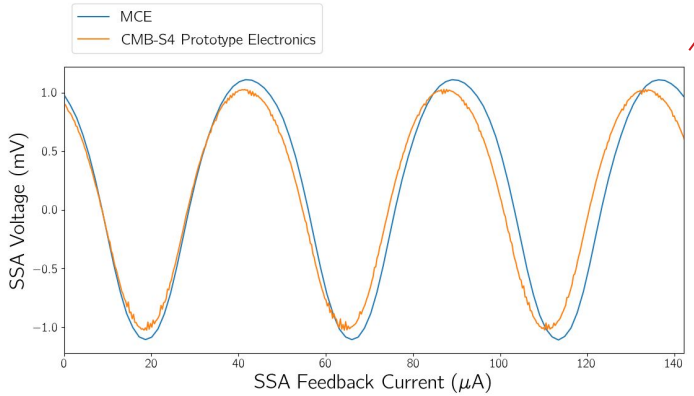
Next prototype run planned (US procurement, CEA vendor management and measurements).

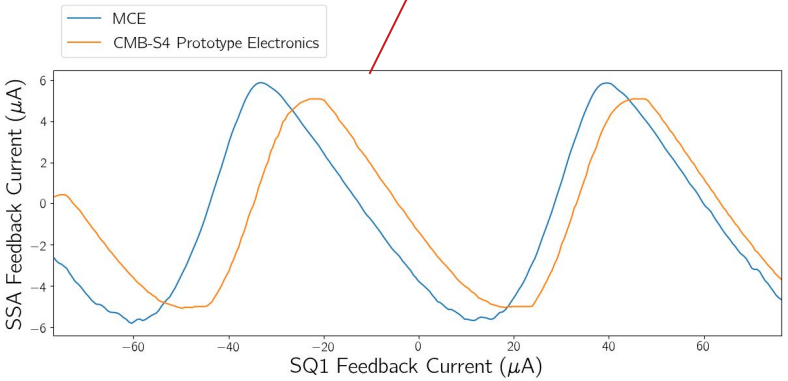
Prototype Warm Electronics Modules

- Started with higher noise than requirements permit. Conducting tests with modular scheme for component-level replacement and A/B testing to systematically build and validate performance model. *(See David Goldfinger fireslide)*
- SQUID tuning functionality and 4K PID/lock-in online. 100mK SQUID PID/lock-in next.
- Able to reproduce 100mK and 4K SQUID response curves from MCE (legacy) electronics.
- Rudimentary data streaming implemented









Exploring Drop-In ASIC For Analog Front-End With IN2P3/France

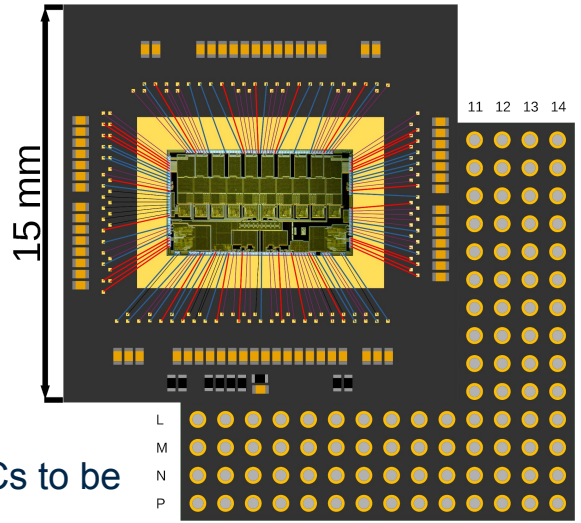
ASIC designed for Athena (APC) with 2 readout channels per chip.

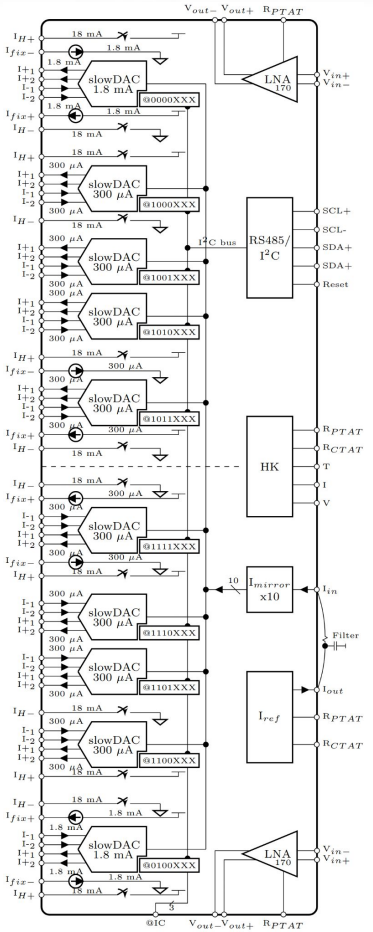
Potential drop in for: **300K LNA, 4K SSA bias, 100mK SQ1 bias**

- Differential
- Low 1/f noise
- Thermal drift compensation

Exploring form factor (LPSC + APC) and compatibility with proto electronics:

- **BGA-like packaging** and integration
- Design of a **daughter board** with 4 ASICs to be integrated in proto electronics.





Near-Term Plans (FY23)

- *Programmatic*
  - Continue to document requirements and interfaces, and increase design maturity
  - Prepare for subsystem conceptual design review
- *100mK Readout Module*
  - Complete component-level designs and fabrication of boards, wiring chips and cable interfaces for 100mK Readout modules for 2-level multiplexer system.
  - Integrate 2-level MUX chips and SSA from NIST and test 100mK modules in cryostat with MCE electronics
- *Detector Module interface*
  - Order, receive and test new superconducting flex cables
- *300K Prototype electronics*
  - Component evaluation for 300K Readout electronics module
  - Testing with analog front-end ASIC when available
  - Perform performance tests of 300K electronics on cryostat

Summary

- Substantial progress on equipping detector teststands with readout.
- Revisions under way for reduced wire-count 80-row readout with 2-level multiplexer and faster second-stage (4K) SSA. Boards, wiring chips etc. being updated accordingly.
- Awaiting new multiplexer and SSA devices from NIST to test and validate
- Started new international partnerships for joint R&D and exploring potential project work scope.
  - Superconducting flex cable
  - Analog front-end
- First prototype of warm electronics functional; working out component-level, empirically-validated noise model to inform next spin.