Detector Status

Brenna Flaugher

CMB-S4 Collaboration Meeting
April 3-6, 2023

Proposed Outline

- Subsystem Team
- Scope and changes due to AoA
- Technical overview/progress/status
- Near-term plans
- Summary

Detector WBS Structure Is Based On Fabrication Sites And Captures Technical Expertise In L3 Manager Roles

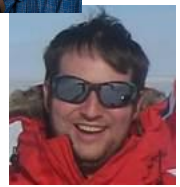
1.03 DETECTORS

*Brenna Flaugher** (FNAL)
John Joseph (LBNL)

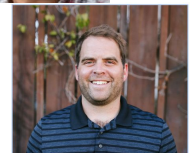
- **1.03.01 Detector Management** — John Joseph (LBNL)
- **1.03.02 ANL Wafer Fabrication** — Clarence Chang (ANL)
- **1.03.03 SLAC Wafer Fabrication** — Dale Li (SLAC)
- **1.03.04 JPL Wafer Fabrication** — Jamie Bock (JPL), Roger O'Brient (JPL)
- **1.03.05 NIST Wafer Fabrication** — Shannon Duff (NIST)
- **1.03.06 LBNL/SeeQC Wafer Fabrication** — Aritoki Suzuki (LBNL)
- **1.03.07 UCB/Marvell Wafer Fabrication** — Adrian Lee (UC Berkeley)









AoA Alt1 requires 363 (instead of 471) modules

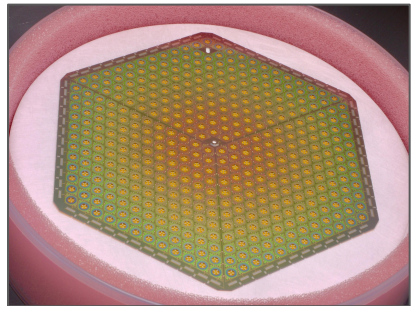
- SATs: 108 modules, 8 frequency bands
- LATs: 255 modules, 7 frequency bands

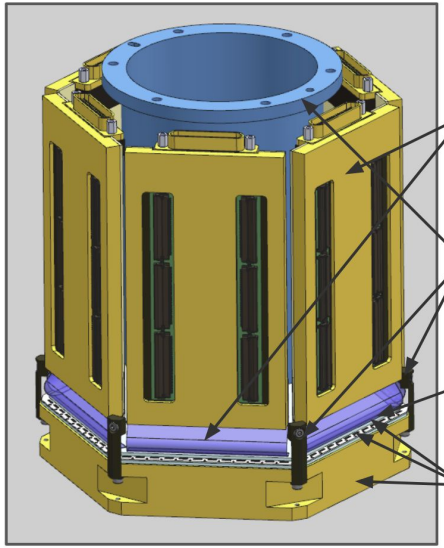
Impact of AoA 1:

- Reduced number of SAT wafers/modules (108)
- Reduced production time required by ~ 1 year to ~ 3 years

Still a lot of wafers and modules:

With ~10% overage ~ 400 wafers/modules
AND ~67% yield ~ 586 wafers/modules





CMB-S4 Detector Fabrication Group (CDFG) Facilitates Collaboration

- CDFG Charter: create a single, collaborative group to engage CMB-S4 detector experts during the design and fabrication phases of the CMB-S4 detectors. CDFG is an advisory group and meets weekly or bi weekly since Jan. 2020 - **Wednesdays 12-1 CDT**

- CDFG Chair - Brenna Flaugher (interim Detector L2 scientist), Membership consists of representatives from ANL, JPL, LBNL-Seeqc, NIST, Stanford-SLAC, UCB (most are also L3 managers), WBS 1.04 Readout and 1.05 Module L2 leads

- CDFG Goals:
  1) address intellectual property and conflict of interest concerns - Done
  2) fabricate prototype detectors which meet preliminary draft criteria (CDFG-wafers) and full CMB-S4 prototypes - in progress
  3) create single, coherent detector fabrication plan engaging multiple sites (strawperson in next slides)

Strawperson Detector Fabrication Plan Uses 6 Sites To Reduce Risk

- Each detector type fabricated by at least 2 sites to reduce risk of single point failure
- Develop 6 sites (SLAC starts FY25/26), maximize flexibility to capture existing resources and expertise; minimize need to hire/train new people or procure new equipment
- Build on existing experience and relationships between Labs, Universities and Commercial
- July 2021 request for information (RFI) sent to all fab. sites: production rates, cost, equipment needs, potential for ramp up beyond current rate
- To protect proprietary information we calculated an average rate and cost; used in P6
  - Average rate ~2 science grade wafers per month per site; some sites indicated additional capacity available
  - Average cost per science grade wafer calculated from RFI response is $92K
- Project will optimize the strawperson fabrication plan based on risk, cost and schedule as we proceed through prototype and pre-production stages

Strawperson Production Fabrication Plan Lasts ~3 Years (AoA -1)

- Production sequence and quantities adjusted based on AoA. Incorporation into P6 is in progress
- Total detector production cost uses the average cost per wafer and the distribution across sites in this plan
- Plan to reoptimize Fab site assignments based on performance, risk, cost and schedule at least annually

sheet (pin/slot inc)		Number Wafers	name
12	SAT 30/40GHz	12	SAT LF
27	LAT 20GHz	4	LAT ULF
48	LAT 30/40GHz	25	LAT LF
145	SAT 85/145	36	SAT MF1
167	SAT 95/155	36	SAT MF2
430	LAT 90/150	162	LAT MF
467	SAT/LAT 225/278	88	SAT/LAT HF

Dates are based on starting production with CD2/3a (26/27)

Focused R&D on SAT MF2, LAT MF and LF:

- Need the most of these
- Reduced complexity for module assembly and testing

Each year assess performance and redistribute

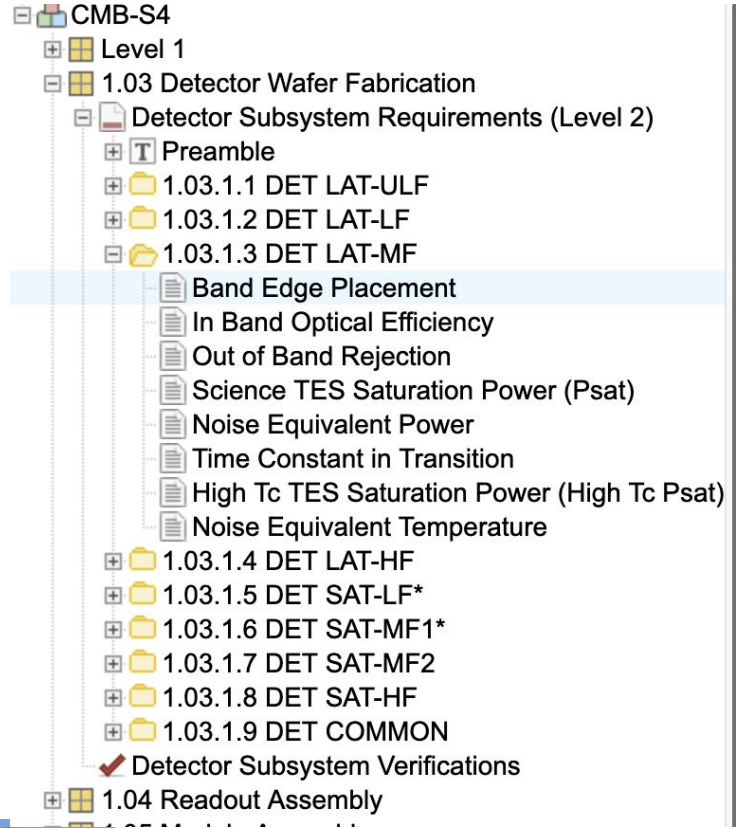
Science Grade Wafers	Years are approximate dates							
	2026		**2027**		**2028**		**2029**	
Site 1 = ANL	2	9	10	12	12	12	12	12
Site 2 = JPL	2	10	6	12	12	12	12	12
Site 3 = SEEQC	2	10	15	8	12	6	12	12
Site 4 = NIST	2	10	12	12	14	8	11	
Site 5 = SLAC	2	10	12	12	12	4	4	6
Site 6 = Marvell	2	4	4	4	4	2	5	7
Total Science Grade	**12**	**53**	**59**	**60**	**66**	**44**	**56**	**49**
~ Number of wafer modules to test	**18**	**78**	**87**	**88**	**97**	**65**	**82**	**72**

Detector Requirements Based On Measurement Requirements

Fabrication sites monitor processing, but **full detector performance can only be verified in module testing.** Key dark, optical, and noise requirements are captured in JAMA.

Requirement	Origin	Driver	Validation
Physical, Thermal, Electrical	Interfaces Flowdown	Detector Layout must meet mechanical, electrical, and thermal interfaces between the detectors and readout (flex cable, bond pads) and module components (mechanical, coupling, etc)	Visual inspection, Warm continuity checks. Process monitoring at each fabrication site.
Detector Dark TES Properties	Flowdown	Electro-thermal properties (e.g. Tc, saturation power, loop gain) of the TES need to be within an acceptable range to meet required instrument sensitivity.	Dark tests of in-process test structures and of every wafer in an assembled detector module at 100 mK.
Detector Optical Performance	Flowdown	Efficiency and frequency response needs to be within an acceptable range to meet required instrument sensitivity (e.g. band edges, uniformity)	Mm-wave/optical tests of single pixels and of each detector wafer in an integrated module at 100 mK.
Integrated Sensitivity	Flowdown	Sensitivity (efficiency, noise, yield, etc.) of integrated module (with readout) depends on sensitivity of detectors, and needs to meet required instrument sensitivity.	Dark and optical measurements of every pixel in a detector module at 100 mK operating temperature.
Fabrication rate and yield	Schedule	Detector fabrication rate and yield drive project cost and schedule. Optimization of project fabrication plan (assignments to each site)	Fab. Site QA and Module testing results, cost and schedule performance

Key Detector Requirements And Ranges Are Identified (Example Below, Details In John Ruhl's talk)



Band Edge Placement

Subsystem Requirement (Level 2) • Version 7

PROJECT ID:
CMBS4-DET-411

GLOBAL ID:
GID-66975

NAME:
Band Edge Placement

DESCRIPTION:
The Band Edge requirements define the band edges of the RF filters on the LAT-MF detector wafer. The Band Edges are defined as the frequencies of the band pass filter that provide 50% transmission relative to the average over the band, (Assuming ideal horn/OMT design)

Band Pass LAT-MF_1
Lower Pass Band Edge: 77 GHz, +/- 3%
Upper Pass Band Edge: 106 GHz, +/- 3%
Center Frequency: 91.5 GHz Nominal and not specified as a requirement

Band Pass LAT-MF_2
Lower Pass Band Edge: 128 GHz, +/- 3%
Upper Pass Band Edge: 169 GHz, +/- 3%
Center Frequency: 148.5 GHz Nominal and not specified as a requirement

R&D Has Made Great Progress with limited funding

2020/21:

- Focused early R&D on developing multiple fab site capabilities:
  dual Tc TES, OMT/ DRIE, etc to improve fabrication flexibility and reduce risk.

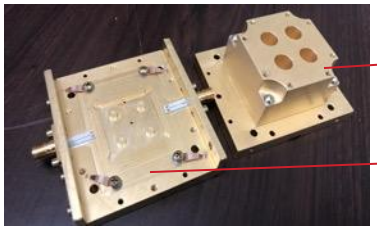
2022/23:

- ANL and SeeQC fabricated CDFG wafers to meet draft requirements and delivered to FNAL: looking forward to first dark tests in flat modules in ~ 2 months
- R&D with test structures and single pixel setups at Fab sites; check single pixel performance against requirements (optical and dark), then move to full array fab.
- Fab sites started development of prototype CMB-S4 wafers:
  - NIST and ANL: LAT MF wafers
  - SeeQC and JPL: SAT MF2
  - UCBerkeley: LAT LF
- Prototype CMB-S4 wafers expected this summer

Argonne Detector Fab highlights

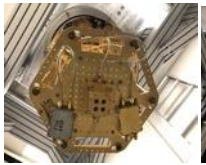
- Measured microstrip loss at 150 GHz & 220 GHz
- Designed and fabricated optical test setup and optical test devices
- Measured the microstrip materials loss by comparing transmission across different line lengths
- Validated that materials have loss similar to what has been demonstrated for previously fielded OMT coupled detectors
  - Measurements are consistent with the loss being dominated by the dielectric. Suggests the Nb layers are good and transmission can be tuned by changing dielectric material

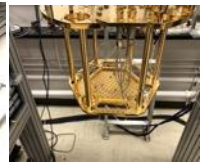
Optical test hardware



Feedhorns

Backshorts



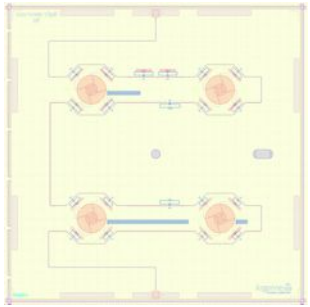


Detector stage

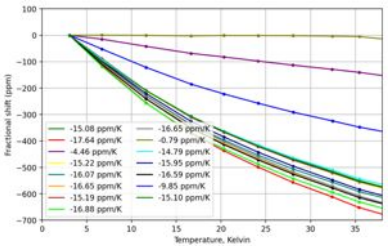
Metal-mesh filters

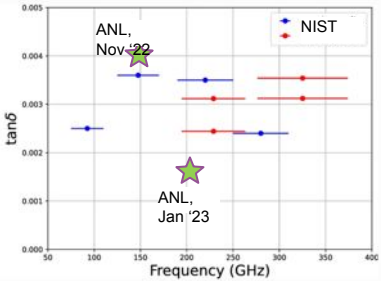
Cryogenic blackbody

Optical measurements



Optical test chip with varying microstrip lengths





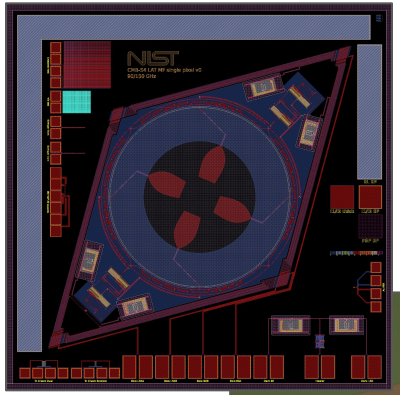
Measured 220 GHz response to a cryogenic blackbody. Shorter lines have larger response. Loss comparable to other OMT detectors

Fig adapted from Hubmayr, J. et al., JLTP 209, 396–408 (2022)

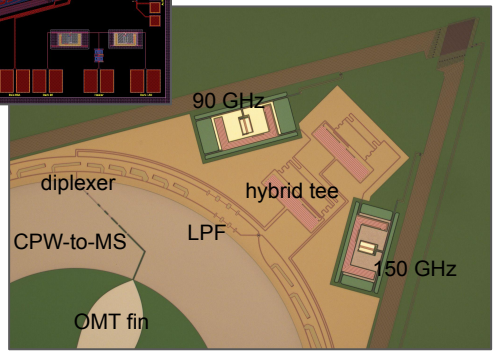
NIST Detector Fab highlights

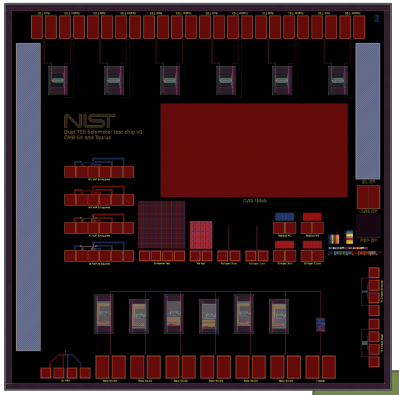
Prepared the LAT MF detector to module ICD (Doc-DB 463)

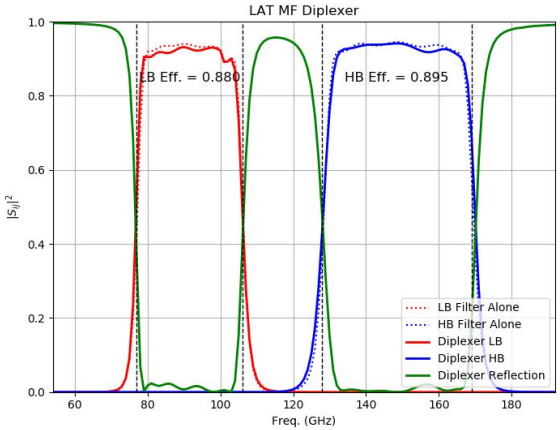
Finalized design and layout for LAT MF prototype single pixel and dual-TES bolometer chip, fabrication ~90% complete



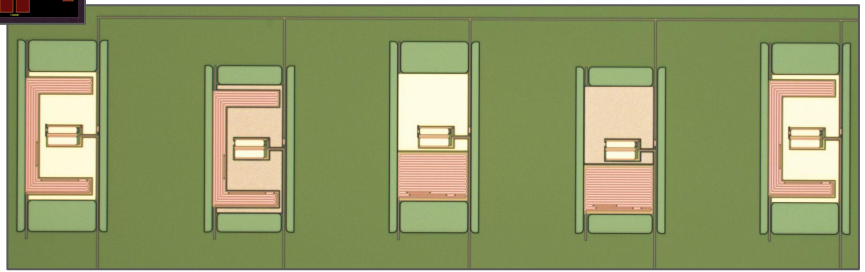
LAT MF prototype single pixel contains full optical pixel and 90/150 GHz dark bolometers



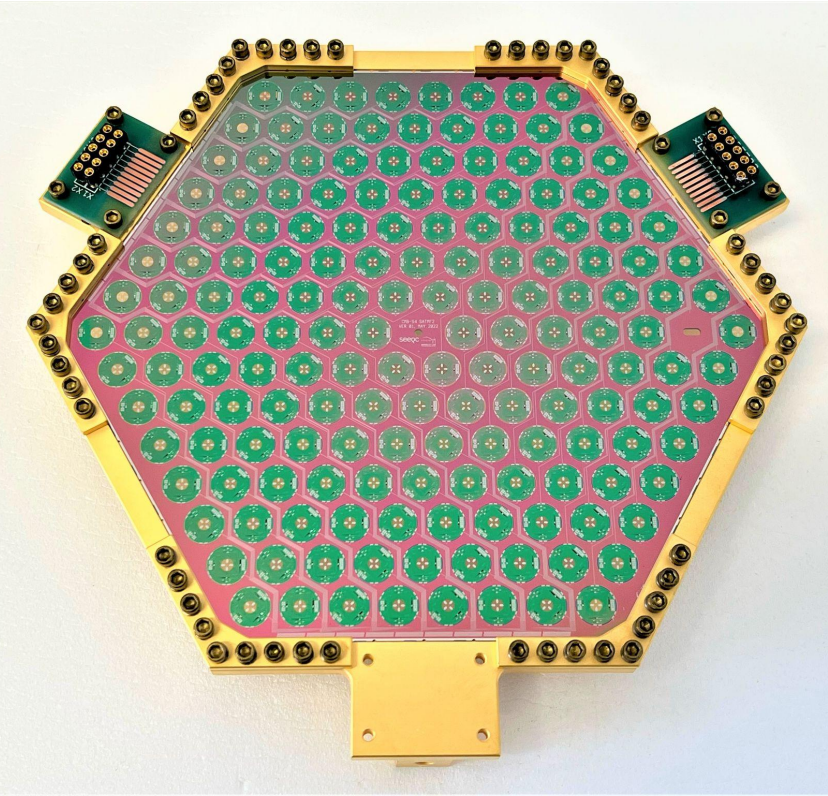


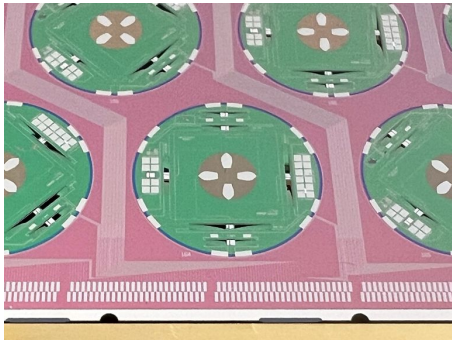


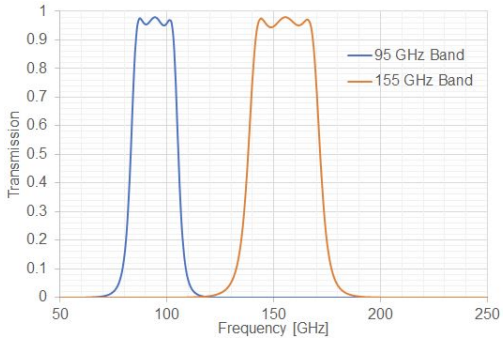
Dual-AlMn-TES bolometer chip has 12 device splits to explore heat capacity, termination, and thermal conductance (5 device splits shown below)



LBNL-SeeQC Detector Fab highlights







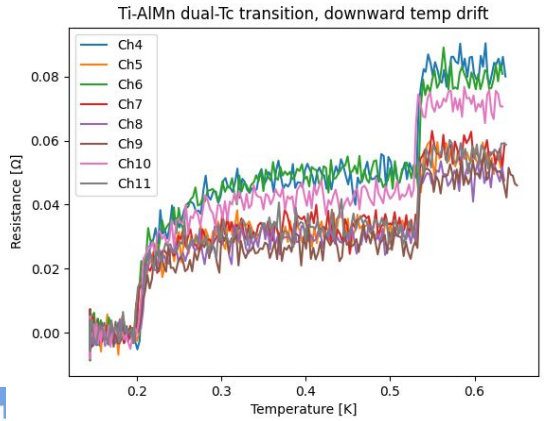
LBNL-Seeqc team coordinated with DRM WBSs to finalize SAT-MF2 design (Doc-DB 837) and ICD (Doc-DB- 839)

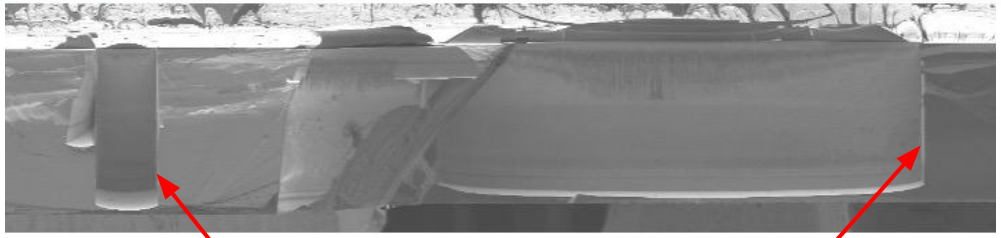
Seeqc completed fabrication of the first SAT-MF2 wafer!

Wafer is mounted in a detector holder to be tested at LBNL soon

JPL Detector Fab highlights

- Preparing to Fabricate SAT MF2 wafers.
  - Most steps similar to BICEP detector recipes
  - Will use deep-UV wafer-stepper lithography
- Finalizing recipes new to S4 process:
  - Backside DRIE etches
  - dual-Tc Ti/AlMn TESes





TES DRIE etch: wall profile is dr/dz=1%

OMT DRIE etch: dr/dz=2% slope

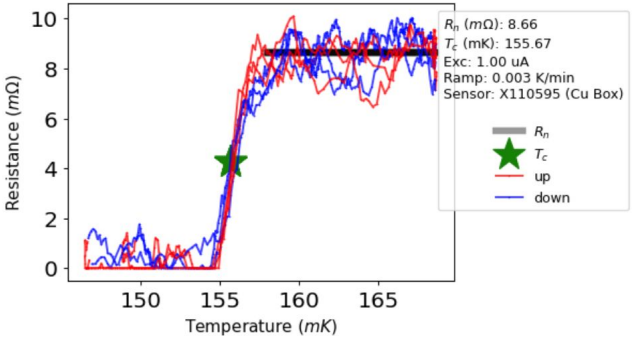
- Above: Backside DRIE etch tests, cleaved and characterized with SEMs. Slopes acceptable.
- Left: resistance vs Temp for dual-Tc Ti/AlMn TESes
  - Measurements show transitions at the expected 200mK, verifying Co-sputtered AlMn recipe.
  - Transitions at 550mK show the expected Titanium transitions
  - Device includes the Nb leads, all film interfaces in the bias leads

UC Berkeley Detector Fab highlights

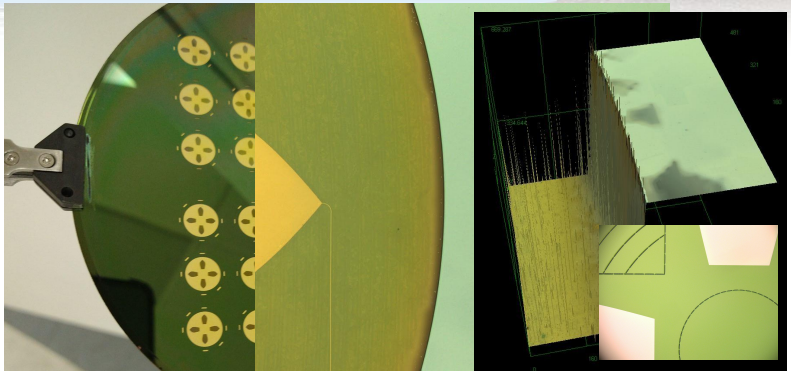
- Completed co-fabrication with SeeQC OMT test wafer for LAT LF with 100% yield
  - Successful DRIE etch of large OMT holes
  - Compatible with final LF bands

- 90% complete with prototype single pixel LF wafer with TES and bolometric seep

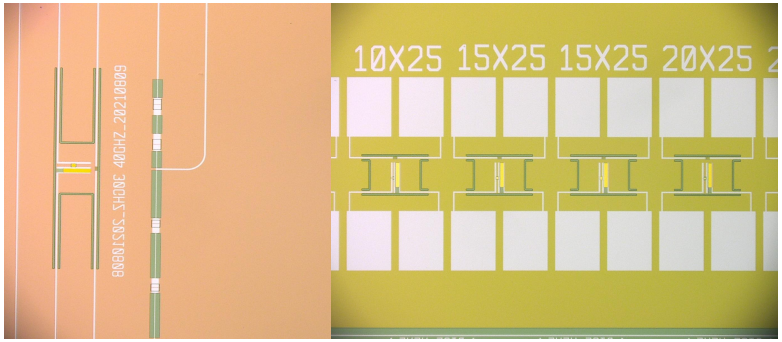
- Demonstrated first Dual TES and science TES transition for CMB-S4



Science TES with 8.6mOhm 156mK

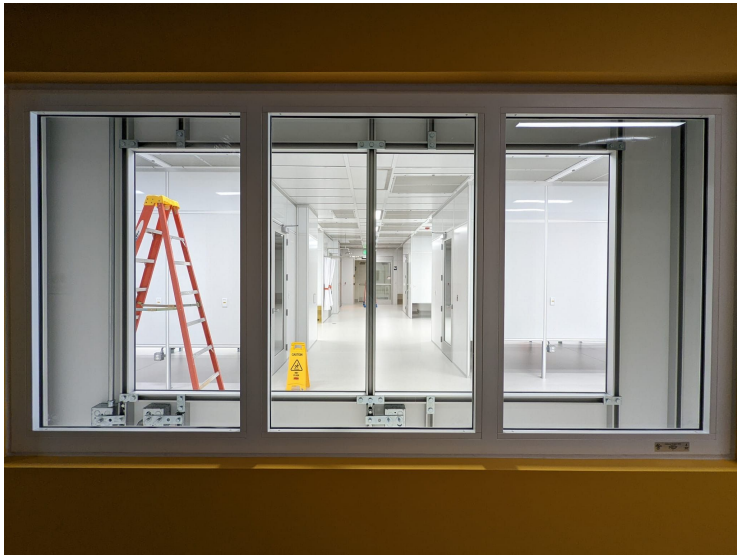


Large OMT Test Wafer + Backside confocal microscopy



Bolometer, wiring, filter, microstrip, cpw, and OMT
Dual TES geometry sweep

SLAC is making great progress on the new building



Next Steps Toward CD-1 Include Testing Prototype Arrays In Modules And Development Of Draft Detector QA Plan

- **FY23 Focus on LAT MF and SAT MF2 Prototype arrays, LAT LF R&D**
  - Follows on FY20/21/22 R&D
  - Testing in modules/feedback on performance has been more difficult than anticipated:
    - Availability of Readout and Rf coupling wafers, assembly/wire bonding challenges… See modules talk
    - Spring 2023 start Dark Tests in Flat modules; up to ~ 80 TES/module
    - Summer 2023 start Optical tests in Flat Modules; up to ~ 80 TES/module
  - Expect to test wafers from at least 2 sites in FY23
  - Begin to develop QA plans/procedures for each site and across all sites

- **FY24/25 Fab site yield, rate, QA, demonstrate performance**
  - Fabricate sequential batches of wafers at each site
  - R&D for other wafer types (HF, SAT MF1) arrays
  - Refine QA plans and procedures
  - Move to new readout when available - enables testing of more TES/wafer
  - Reoptimize fab. plan, cost, schedule and risk assessments

Summary

- Strawperson Detector Fabrication plan has been updated to match Alternative 1;
  - Reduces number of SAT science grade wafers by 108, saving ~ 1 year of wafer production time
  - Risk minimized by using multiple sites
  - Aug. 2021 RFI feedback is basis for cost and schedule assumptions
  - Incorporation into P6 is in progress

- Early R&D has made great progress; FY23/24 plan is focused on
  - Single pixel and test structure studies for process development
  - Delivery of CMB-S4 prototype detector arrays from multiple sites
  - Finalizing LAT LF design, single pixel and test structure studies
  - Refining designs based on feedback from module testing (with early readout)
  - Development of draft QA plans

- Longer term steps include
  - Demonstrating yield, cost and schedule performance
  - Development of QA plans
  - Refining cost/schedule/risk