Detectors [WBS 1.03] Status

John Joseph
L2 CAM - Detectors (1.03)

CMB-S4 Collaboration Meeting
May 9-13, 2022

Who we are

1.03 DETECTORS

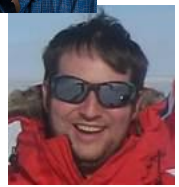
*Brenna Flaugher** (FNAL)
John Joseph (LBNL)

1.03.01 Detector Management
John Joseph (LBNL)

1.03.02 ANL Wafer Fabrication
Clarence Chang (ANL)

1.03.03 SLAC Wafer Fabrication
Dale Li (SLAC)

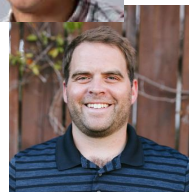
1.03.04 JPL Wafer Fabrication
Jamie Bock (JPL)
Roger O'Brient (JPL)



1.03.05 NIST Wafer Fabrication
Shannon Duff (NIST)

1.03.06 LBNL/SeeQC Wafer Fabrication
Aritoki Suzuki (LBNL)

1.03.07 UCB/Marvell Wafer Fabrication
Adrian Lee (UC Berkeley)
Ben Westbrook (UC Berkeley)



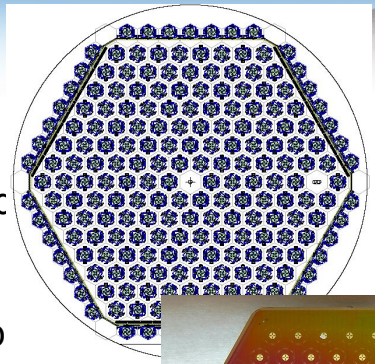
Where are we now? Where are we going?

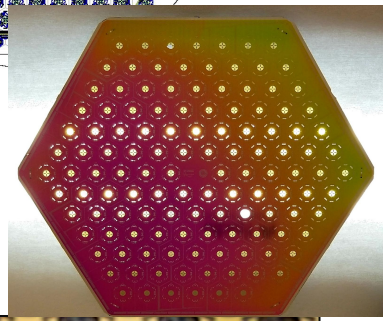
- High level accomplishments:
  - Requirements have been captured in JAMA and completely updated
  - Req. refinements will continue on until they are completed
  - ICDs are in the development stage for all of the current designs
  - ICDs will be transferred to JAMA when the tool is ready for that step

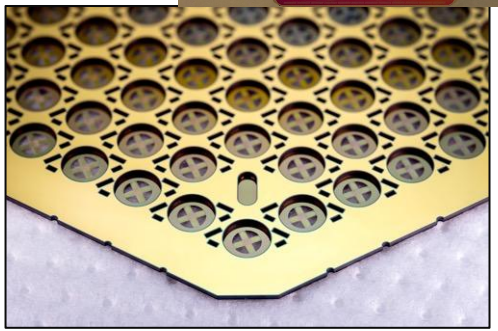
- FY22 plan is to focus on building S4 Detector Arrays
  - LBL/SeeQC & JPL: SAT MF2
  - NIST: LAT MF
  - UC Berkeley: LAT LF

Link to plan: https://cmb-s4.atlassian.net/jira/plans/reports/YZaI3

- Slides will cover recent progress and work we plan to do this year at each fabrication site

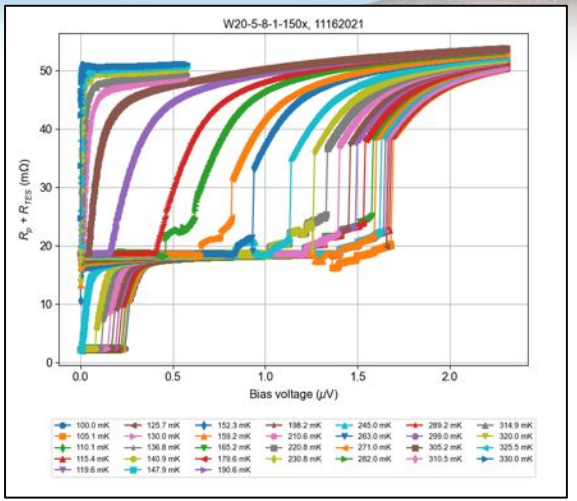


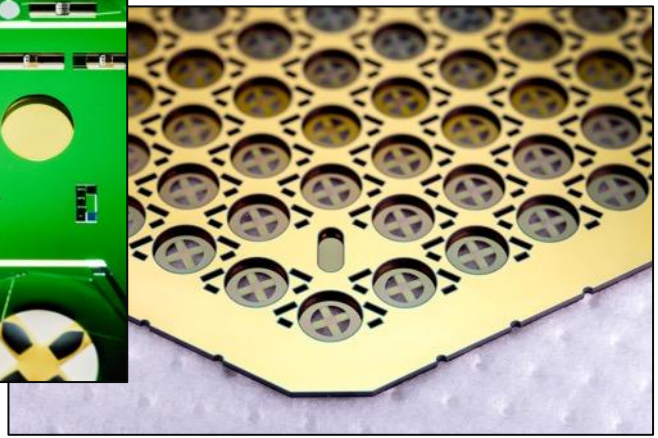


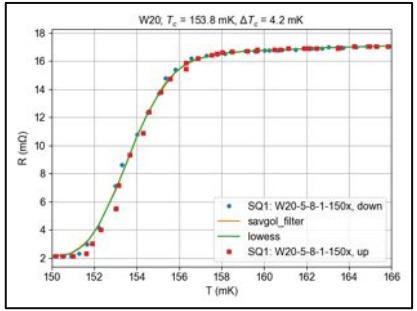


Recent Progress – Argonne

- Completed fabrication of CDFG RFI arrays in early Fall
- Initial measurements show:
  - Tc, Rn and Psat close to desired values for both science and calibration TES
  - Calibration TES transition is shallower (as designed) and can be stably operated

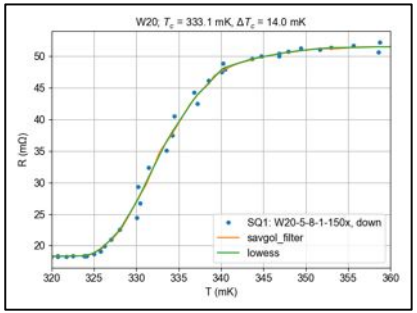






R(T) for Science TES

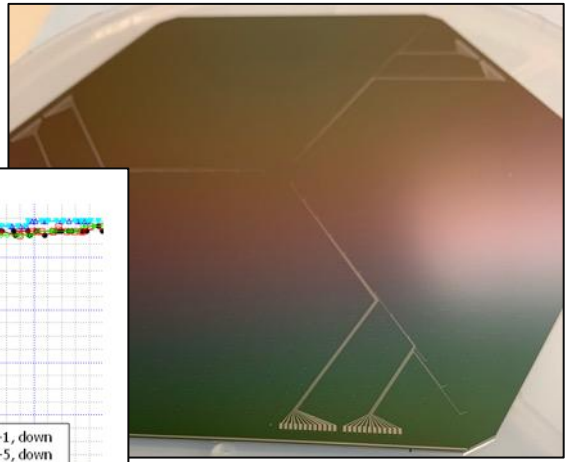
R(T) for Calibration TES

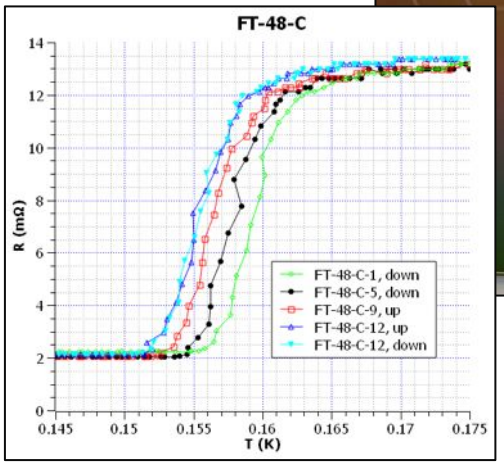


Recent Progress – Argonne

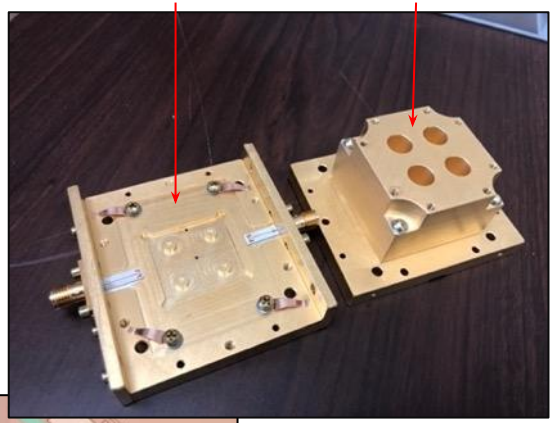
- Following up CDFG RFI tests with materials studies of key components

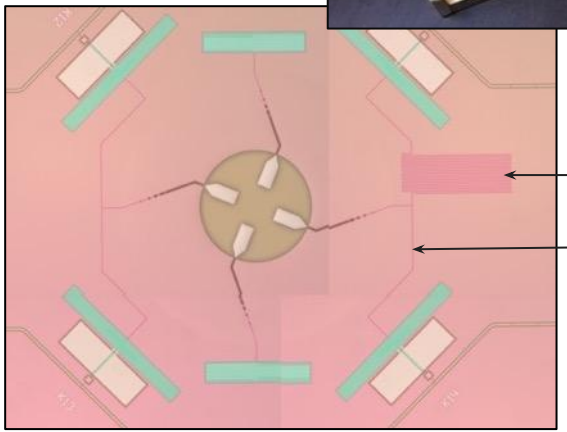
TES uniformity studies





Optical component studies



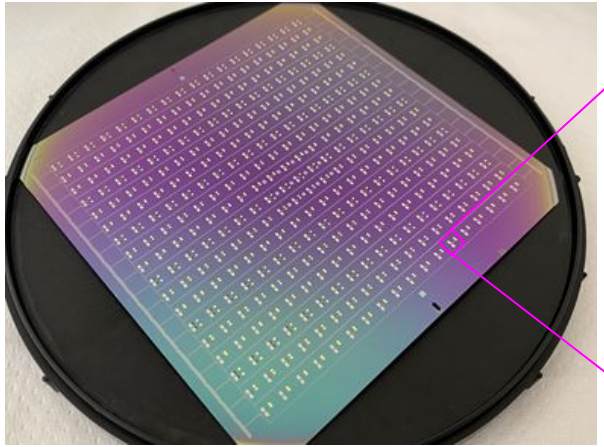


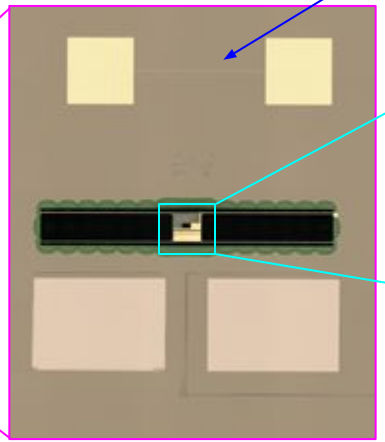
Argonne Deliverables Will Focus on Microstrip Materials and Fabrication Process Development

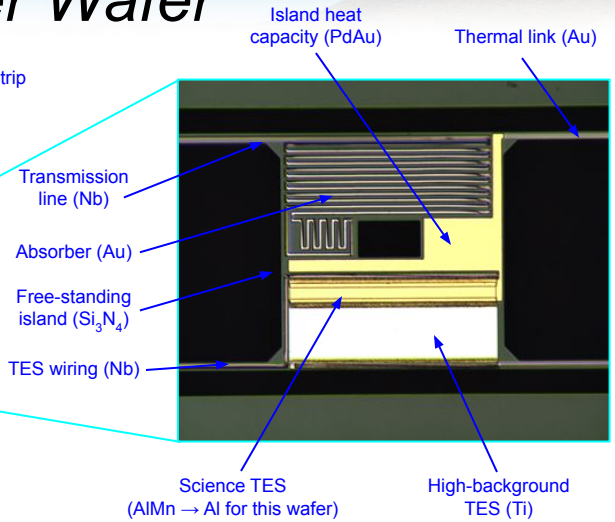
#	Issue	Status	Target st...	Start date D	Due date D
1	DRM-1 1.03 Detectors	IN PROGRESS		01/Mar/22	
	DRM-33 1.03.01 Detector Management	IN PROGRESS		01/Mar/22	28/Apr/23
	DRM-4 1.03.02 ANL Wafer Fabrication	BACKLOG		01/Apr/22	28/Apr/23
	DRM-54 Studies of microstrip materials and fabrication processes	IN PROGRESS	01/Apr/22	02/May/22	28/Apr/23
	DRM-55 First iteration studies of microstrip materials properties and i...	IN PROGRESS	01/Apr/22	02/May/22	31/Oct/22
	DRM-56 Second iteration studies of microstrip materials properties an...	BACKLOG	01/Jul/22	01/Nov/22	28/Apr/23

Recent Progress - JPL *Ti TES Bolometer Wafer*

TES Test Wafer

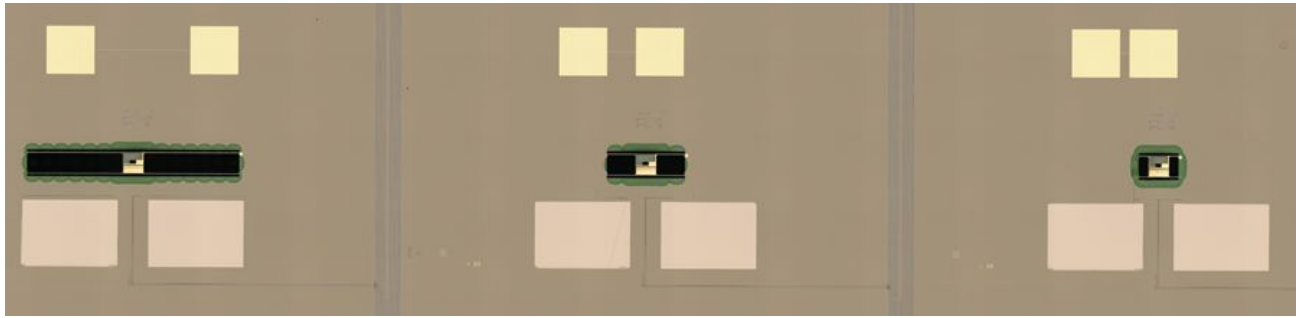




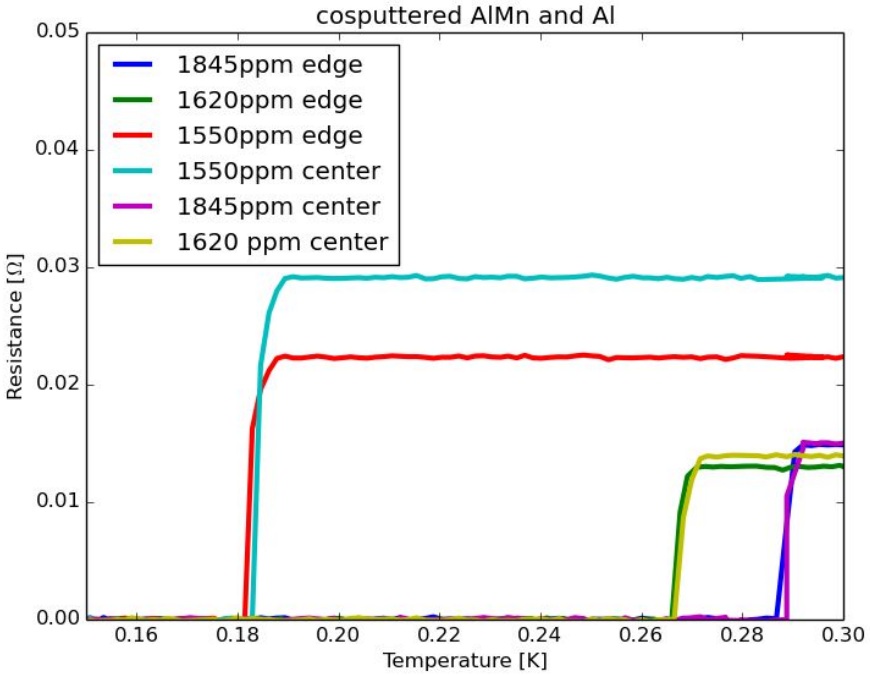


- Ti = High-Tc TES
- AlMn = Science TES
- AlMn → Al for first wafer
- Uses Au link for low □
- 18 x 18 x 2 array
- 27 bolometer types
- 3 Gs x 9 island geometries
- Fabrication completed
- Wafer going into test

LF low-G geometry | MF mid-G geometry | HF high-G geometry



Recent Progress - JPL *AlMn TES Development*

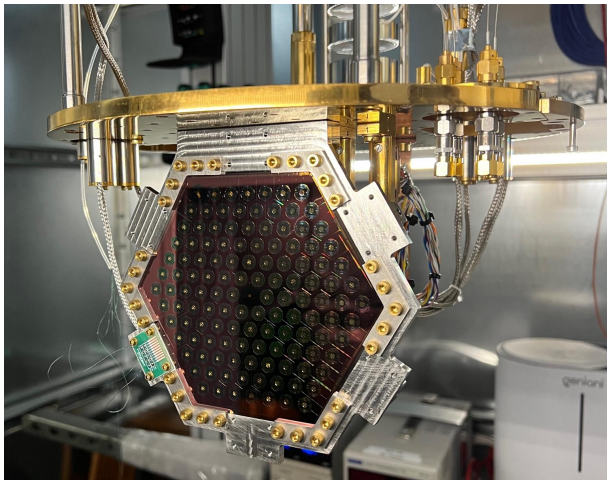


- Films are co-sputtered confocally from a pure Al target and a 2500ppm AlMn target.
- Adjust Mn concentration with relative sputter powers
- Annealed at 200C for 10 min
- Targeted 180mK and 270mK. Close to target values with current recipes.
- Will order targets with target concentrations.
- Consistent Tc from center to edge
- Variations in plot from bonding variations
- Center to edge resistivity varies by 20% (non-contact inductive measurements)
- Deposition rates lithographically characterized
- RRR~2
- Stress is 100-150MPa, compressive.

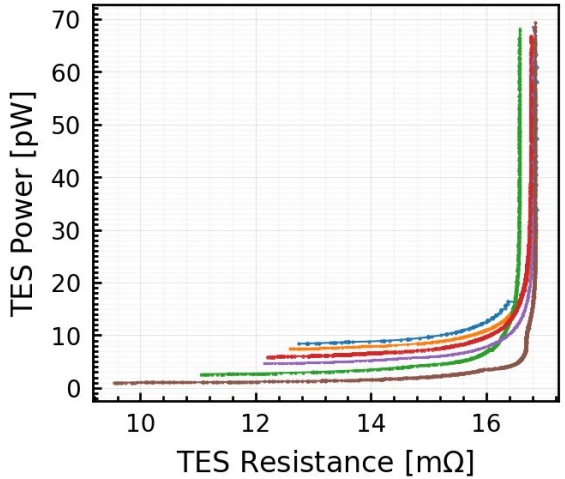
JPL/CalTech is Developing an S4 Level SAT MF2 Detector Wafer to Deliver to MAT

#	Issue	+ Create issue	Status	Target st...	Start date D	Due date D
1	DRM-1 1.03 Detectors		IN PROGRESS		01/Mar/22	
	DRM-6 1.03.04 JPL Wafer Fabrication		IN PROGRESS		02/May/22	28/Apr/23
	DRM-46 Confirm interfaces to SAT MF2 wafer		IN PROGRESS	02/May/22	02/May/22	31/May/22
	DRM-47 SAT MF2 Bolometer cell layout		BACKLOG	01/Jun/22	01/Jun/22	30/Jun/22
	DRM-48 SAT MF2 Wafer Layout		BACKLOG	01/Jul/22	01/Jul/22	31/Aug/22
	DRM-49 Test fixture design		BACKLOG	01/Sep/22	01/Sep/22	23/Sep/22
	DRM-50 SAT MF2 Wafer Fabrication		BACKLOG	01/Sep/22	01/Sep/22	01/Feb/23
	DRM-51 Assemble wafer into test fixture		BACKLOG	09/Feb/23	06/Feb/23	28/Feb/23
	DRM-52 Optical testing SAT MF2		BACKLOG	01/Mar/23	01/Mar/23	28/Apr/23

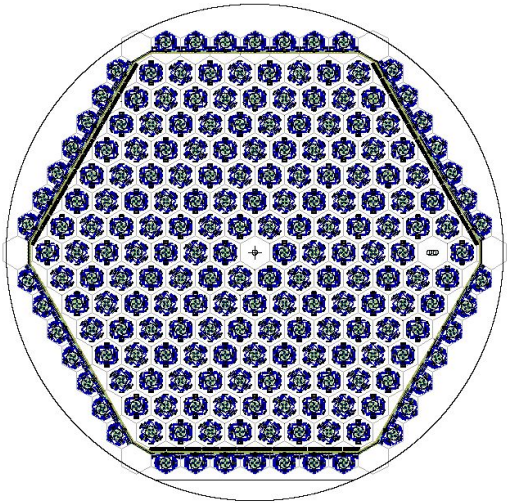
Recent Progress – LBNL/Seeqc



CDFG wafer test at LBNL



R-P curves at different Tb



SAT-MF2 design

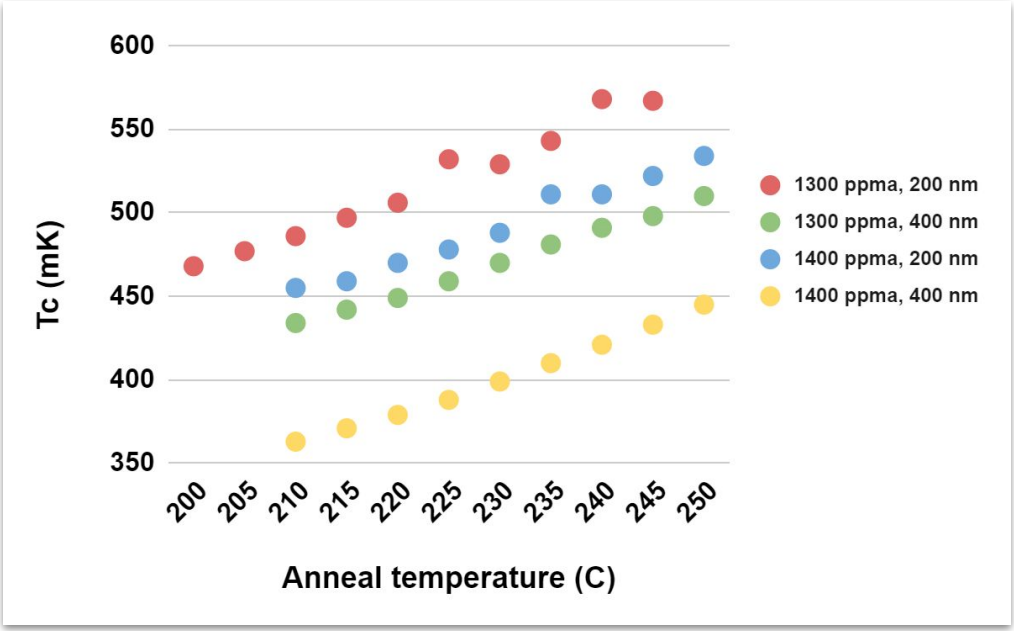
- CDFG mechanical wafer shipped to FNAL
- CDFG “SAT-MF like” wafer with Dual Tc TES fabricated and tested – ship to FNAL soon
- Improved quality assurance processes – Warm and cryogenic tests at Seeqc and LBNL
- Advanced design of the SAT-MF2 wafer

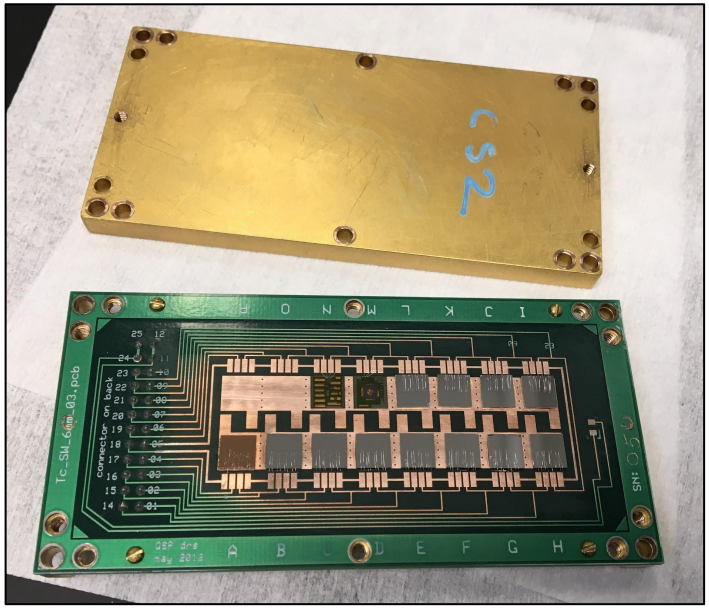
LBNL/Seeqc is Developing an S4 Level SAT MF2 Detector Wafer to Deliver to MAT

#	Issue	+ Create issue	Status	Target st...	Start date D	Due date D
1	DRM-1 1.03 Detectors		IN PROGRESS		01/Mar/22	
	DRM-8 1.03.06 LBNL/SeeQC Wafer Fabrication		IN PROGRESS		01/Mar/22	28/Feb/23
	DRM-15 SAT MF2 Design and Layout		DONE		01/Mar/22	29/Apr/22
	DRM-16 Fabricate first articles of SAT MF2		IN PROGRESS	02/May/22	02/May/22	30/Jun/22
	DRM-17 Test SAT MF2 Wafer LBL, deliver to FNAL		BACKLOG	01/Jul/22	01/Jul/22	29/Jul/22
	DRM-18 Design update using FNAL Dark Characterization feedback		BACKLOG	01/Nov/22	01/Nov/22	22/Dec/22
	DRM-19 Fabricate second batch of SAT MF2 wafers		BACKLOG	04/Jan/23	04/Jan/23	28/Feb/23

Recent Progress – NIST

- Developed high-Tc AlMn film for calibration TES
  - Decide to proceed with 200 nm 1400 ppma AlMn for calibration TES

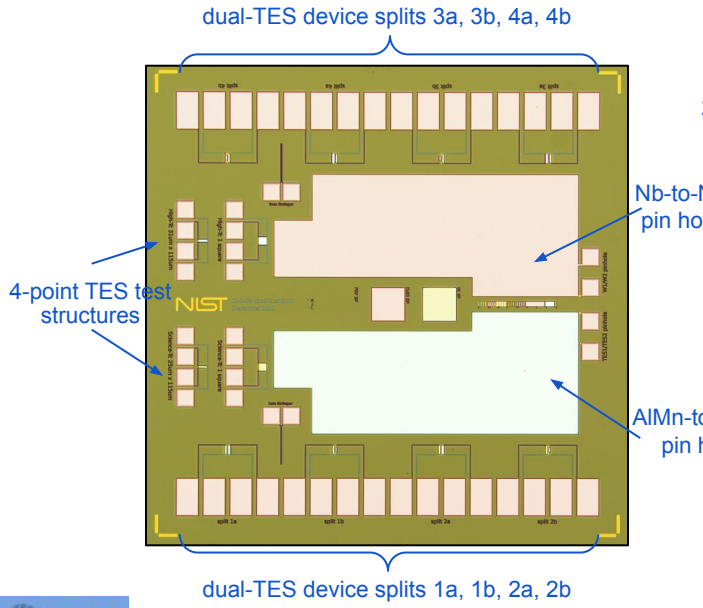


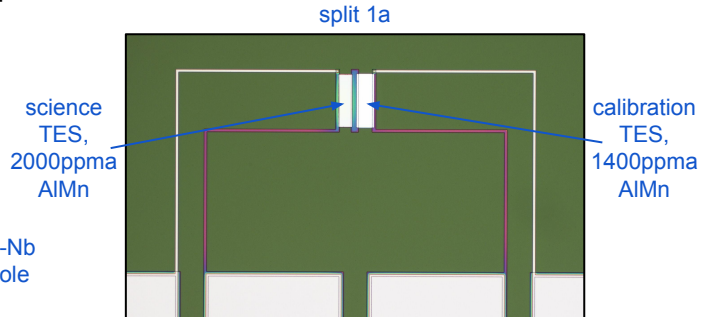


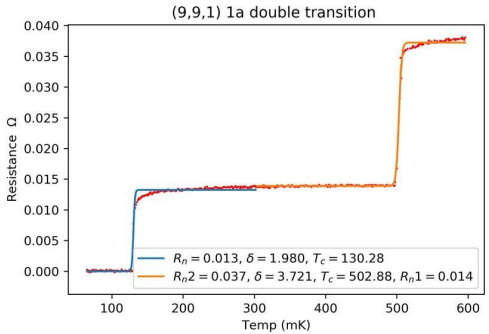
4-point Tc check PCB

Recent Progress – NIST

- Designed and fabricated dual-TES test chip with 8 device splits
  - Measured Resistance vs Temperature for each device split
- Fabricated microstrip resonators to verify dielectric loss is unchanged with modified dual-TES process, measurements forthcoming





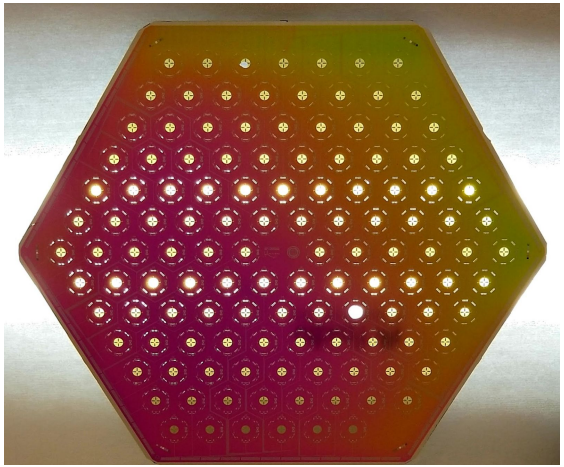


- Science TES and calibration TES close to targeted Tc and Rn values
- Uniform Tc from center to edge demonstrated
- Science TES process heritage from previous CMB experiments with same Tc target

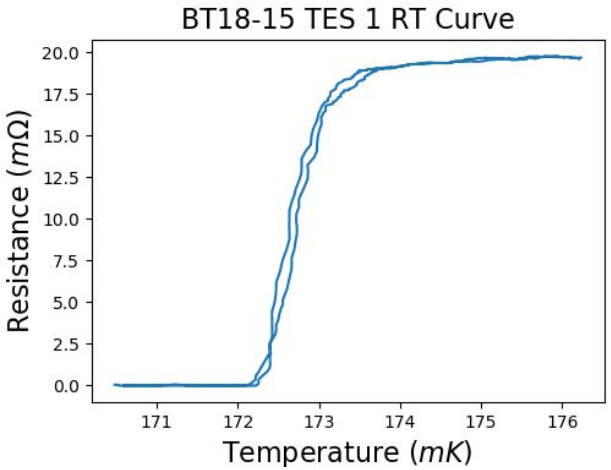
NIST is Developing an S4 Level LAT MF Detector Wafer to Deliver to MAT

#	Issue	+ Create issue	Status	Target st... ↑	Start date D	Due date D
1	DRM-1	1.03 Detectors	IN PROGRESS		01/Mar/22	
	DRM-7	1.03.05 NIST Wafer Fabrication	IN PROGRESS		01/Mar/22	28/Apr/23
	DRM-20	Design/Layout dual TES TC bolometer sweep Chip (LAT MF) ...	IN PROGRESS		01/Apr/22	01/Jul/22
	DRM-21	Fabrication dual TES TC bolometer sweep Chip (LAT MF) and ...	BACKLOG	05/Jul/22	05/Jul/22	25/Aug/22
	DRM-24	Characterization of Bolometer sweeps and pixels chips	BACKLOG	26/Aug/22	26/Aug/22	28/Oct/22
	DRM-25	Design/layout LAT MF prototype arrays	BACKLOG	31/Oct/22	31/Oct/22	22/Dec/22
	DRM-26	Fabrication LAT MF prototype arrays (3 arrays, 1 carry along,...	BACKLOG	04/Jan/23	04/Jan/23	14/Apr/23
	DRM-27	Deliver LATMF Wafers to FNAL	BACKLOG	21/Apr/23	21/Apr/23	21/Apr/23

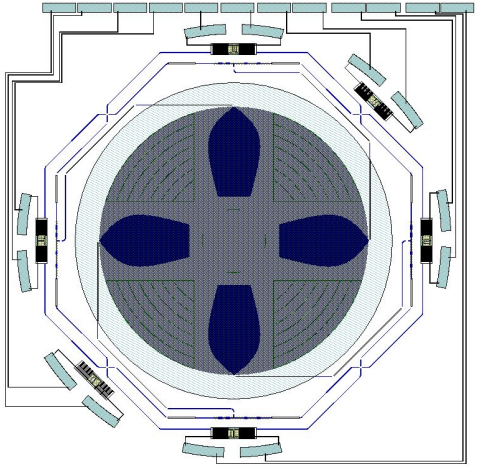
Recent Progress – UC Berkeley



CDFG fabricated at UCB



RT curve for R&D Science TES



Full LF Pixel Design

- CDFG “SAT-MF like” wafer with Single Tc TES fabricated with high yield
- Test TES built with normal resistance and Tc near CMB-S4 targets
- Development of in situ Quality Assurance – DC SQUIDS for mΩ TESs
- Advanced design of single pixel Low Frequency prototypes

UCB is Developing an S4 Level LAT LF Detector Wafer to Deliver to MAT

#	Issue	+ Create issue	Status	Target st...	Start date D	Due date D
1	DRM-1 1.03 Detectors		IN PROGRESS		01/Mar/22	
	DRM-9 1.03.07 UCB/Marvell Wafer Fabrication		IN PROGRESS		01/Mar/22	28/Feb/23
	DRM-10 Design LAT LF Single Pixel		DONE		01/Mar/22	29/Apr/22
	DRM-11 Design LAT LF Single Pixel Wafer		DONE	02/May/22	18/Apr/22	31/May/22
	DRM-12 Fabricate LAT LF Single Pixel Wafer		IN PROGRESS	01/Jun/22	02/May/22	29/Jul/22
	DRM-45 Design complete LAT LF Array		BACKLOG	20/Jun/22	20/Jun/22	29/Jul/22
	DRM-13 Fabricate LAT LF Array		BACKLOG	01/Aug/22	01/Aug/22	23/Dec/22
	DRM-14 Basic Characterization of Single Pixels		BACKLOG	04/Jan/23	04/Jan/23	28/Feb/23

Recent Progress – SLAC: Construction of the Detector Microfabrication Facility

SLAC DMF Construction is on Schedule to Start CMB-S4 Detector Wafer Development in 2023

#	Issue	Status	Target st...	Start date	Due date
1	DRM-1 1.03 Detectors	IN PROGRESS		01/Mar/22	
	DRM-5 1.03.03 SLAC Wafer Fabrication	IN PROGRESS		01/Mar/22	
	DRM-58 Construction of DMF	IN PROGRESS		01/Mar/22	29/Jul/22
	DRM-59 Tool Procurements Complete and Delivered	IN PROGRESS		01/Mar/22	28/Feb/23
	DRM-60 Start of Process Development for CMB-S4 Detectors	BACKLOG	01/Mar/23		