Modules & Testing (MAT) PBDR Overview

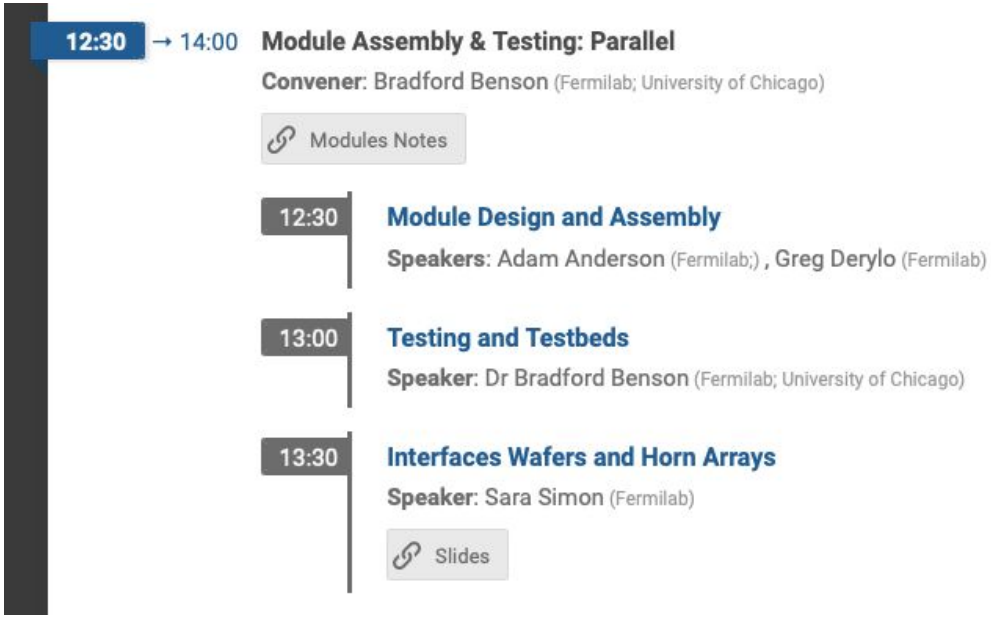
Brad Benson (L2 scientist) for WBS 1.06

Plenary Session, Thursday, March 11, 2021

Outline

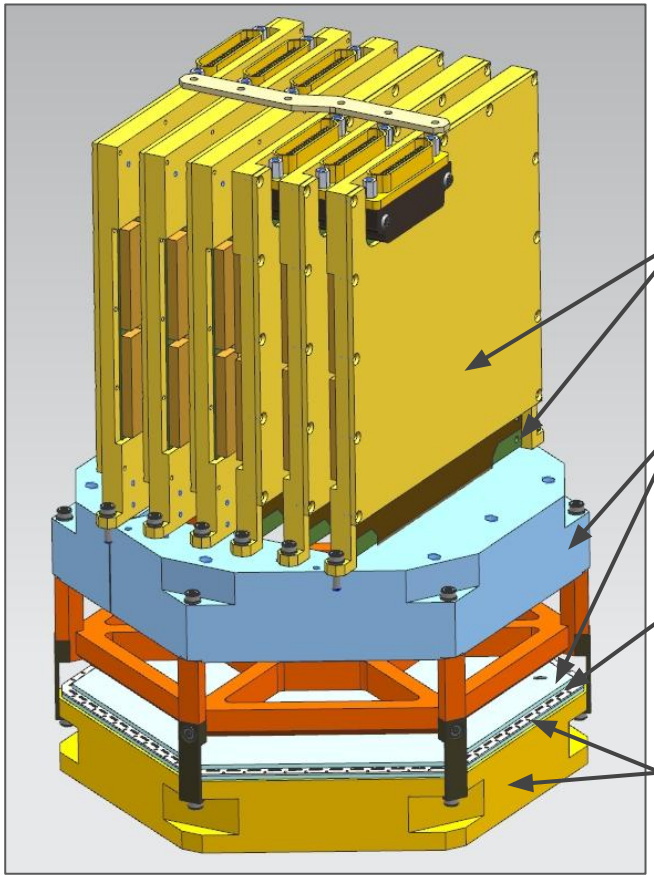
- Modules & Testing (MAT) Scope
- Requirements
  - Detector, Readout, Modules (DRM) FY21 R&D Plan
  - Production Testing
  - SAT, LAT Interfaces
- Design Discussion and Parallels
  - Module design
  - Horn Arrays and Interface Wafers
  - Detector module testing

Thursday 1230-1400 (Pacific)



Module and Testing Scope

1. **Module structure and assembly**
   - Design module structure that holds together DRM components, interfacing with SAT & LAT groups
2. **Optical coupling**
   - Design and build feedhorns and interfaces wafers that form mm-wave integrating cavity for detector.
3. **Integrated module Testing**
   - Perform set of optical and dark tests to validate integrated performance of detector module
   - Characterize and verify wafer performance on pace matching wafer fab through Production.



Module "v1" Design (see A. Anderson's talk)

Flex cable (not shown) — WBS 1.04 Readout

Readout modules — WBS 1.04 Readout

Mounting ring — WBS 1.05 Modules

Backshort wafers — WBS 1.05 Modules

Detector wafer — WBS 1.03 Detectors

Wafer interface plates — WBS 1.05 Modules

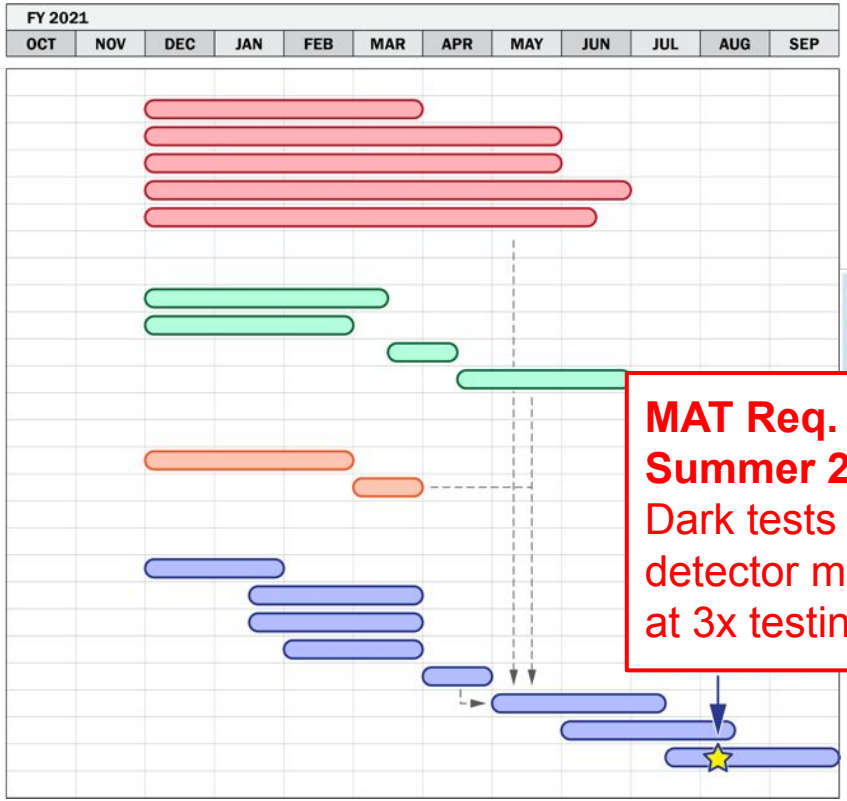
Feedhorns — WBS 1.05 Modules

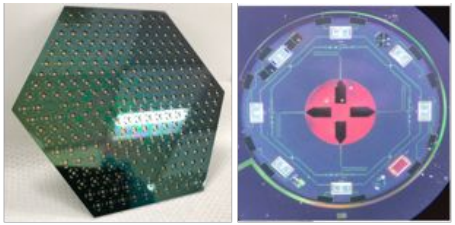
Requirements Overview (CQ2)

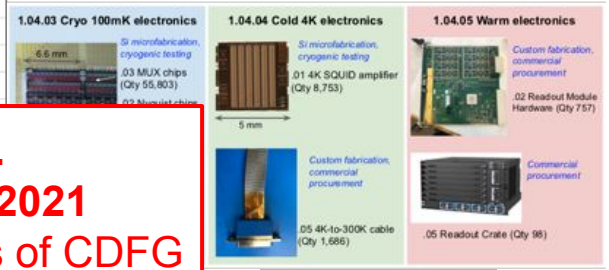
High-level driving requirements include:

Requirement	Trace	Driver	Verification
Measure: Detector Dark Properties	MR 1.1, 1.2, 2.0, 3.0, 4.0	Verify detector wafer. Electro-thermal properties (e.g., saturation power, loop gain) of the TES need to be within an acceptable range to meet required instrument sensitivity.	Dark measurements of every detector wafer in an assembled detector module at 100 mK operating temperature.
Measure: Detector Module Optical Coupling	MR 1.1, 1.2, 2.0, 3.0, 4.0	Verify detector module optical coupling. Efficiency and frequency response of mm-wave coupling to TES needs to be within an acceptable range to meet required instrument sensitivity.	Mm-wave/optical measurements of every detector wafer in an assembled detector module at 100 mK operating temperature.
Measure: Integrated Module Sensitivity	MR 1.1, 1.2, 2.0, 3.0, 4.0	Verify detector module sensitivity. Sensitivity (efficiency, noise, yield, etc.) of integrated module (with readout) needs to be within an acceptable range to meet required instrument sensitivity.	Dark and optical measurements of every detector module with readout at 100 mK operating temperature.
Rate: Assembly and Testing	Schedule	Detector fabrication feedback. Detector module assembly and testing needs to provide measurements at a rate sufficient for detector fabrication development during all phases of project.	

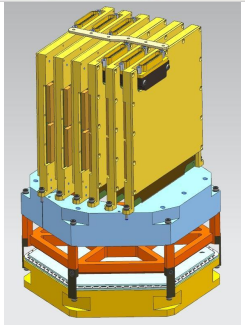
MAT Requirement: R&D / Proto Testing







MAT Req.
Summer 2021
Dark tests of CDFG detector modules at 3x testing sites



See B. Flaugher's Plenary Detector Talk

MAT Requirement: Production Testing

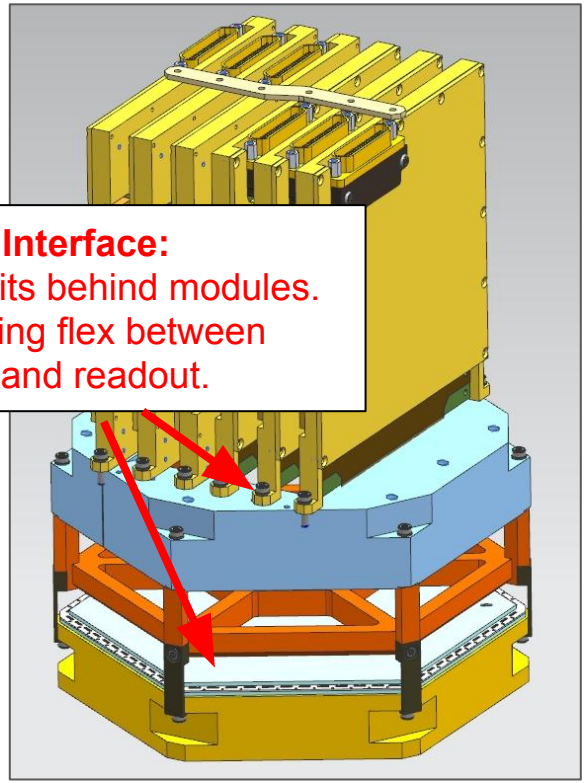
- Rates and detector types discussed with each site and iterated.
- Production rates require minimum ramp-up in capabilities at all sites
- Additional capacity is possible at most sites, with appropriate warning
- Plan to reoptimize based on performance, cost and schedule at least annually

PRODUCTION		Split years into part A and B for transition to new detector type									
	FY23A	FY23B	FY24A	FY24B	FY25A	FY25B	FY26A	FY26B	FY27A	FY27B	Total
Site 1 = ANL	2	8	8	10	10	10	10	8	10	10	86
Site 2 = JPL	2	8	8	8	14	16	16	16	12	6	106
Site 3 = SEEQC	2	8	10	10	16	16	16	16	4	4	102
Site 4 = NIST	2	8	8	8	10	12	14	16	16	14	108
Site 5 = SLAC					8	12	16	11	11	10	68
Site 6 = Marvell	1	3	4	5	4	4	4	4	4		33
Total Science Grade	9	35	38	41	62	70	76	71	57	44	503
~ Number of wafer modules to test (inc. 12% overage and 67% yield)	15	59	64	69	104	117	127	119	95	74	841

MAT Req: Assemble and test ~600 detector modules over 3-year period

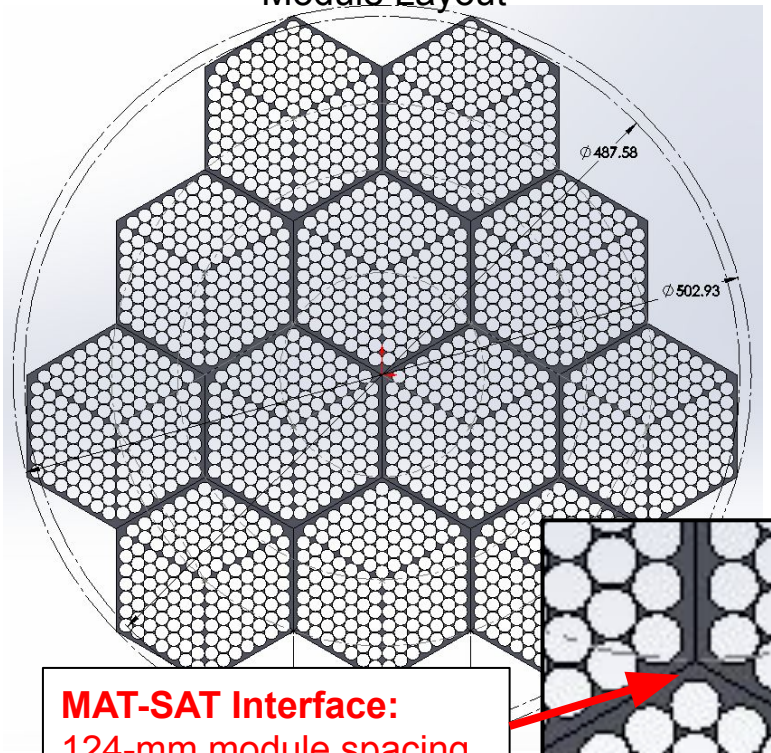
See B. Flaugher's Plenary Detector Talk

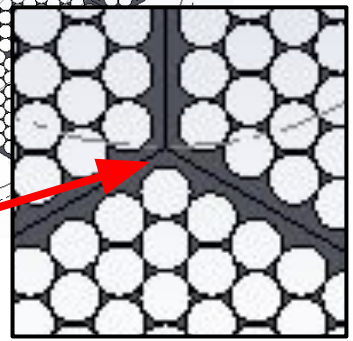
Key Interfaces: Readout+SAT



MAT-Readout Interface:
-Readout box fits behind modules.
-Superconducting flex between detector wafer and readout.

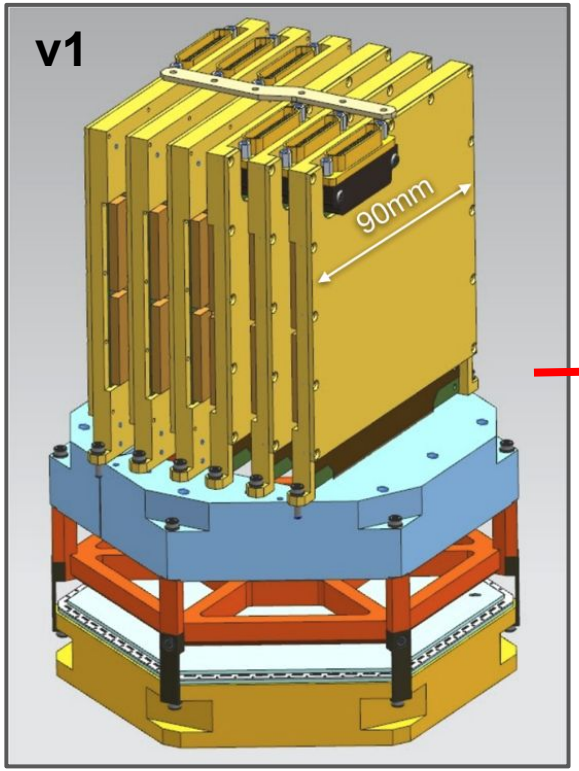
Proposed SAT Detector Module Layout

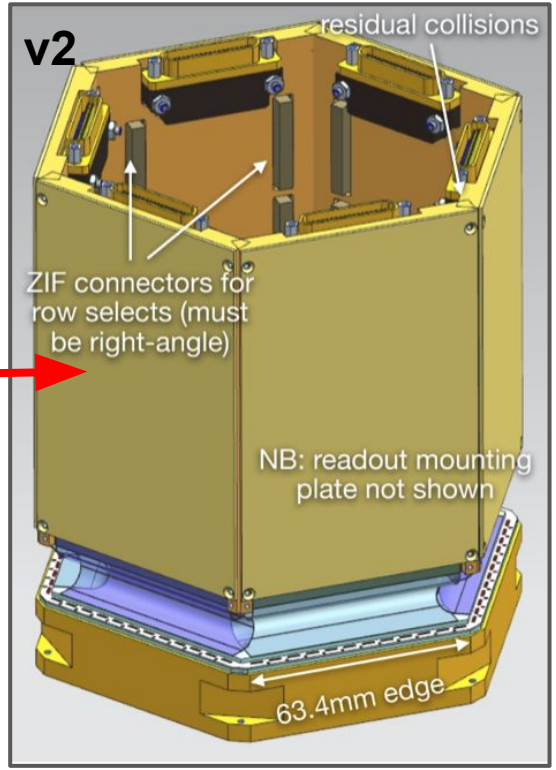


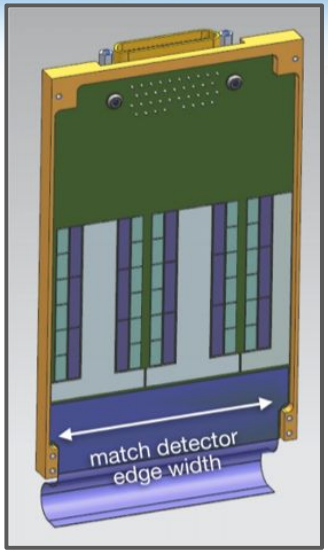


MAT-SAT Interface:
124-mm module spacing

1) Module Design





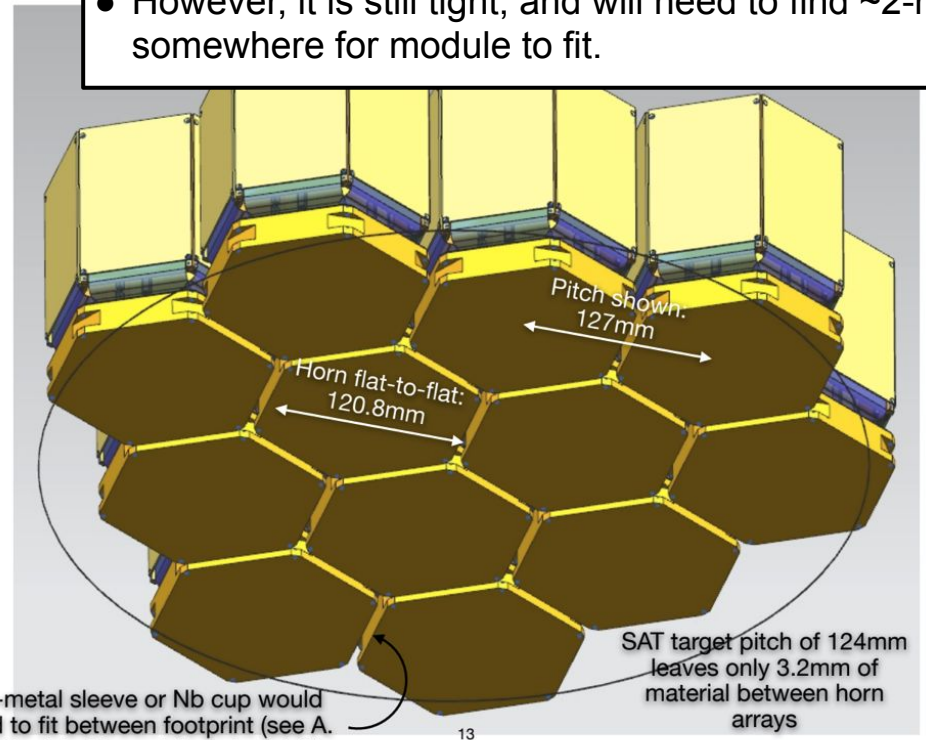


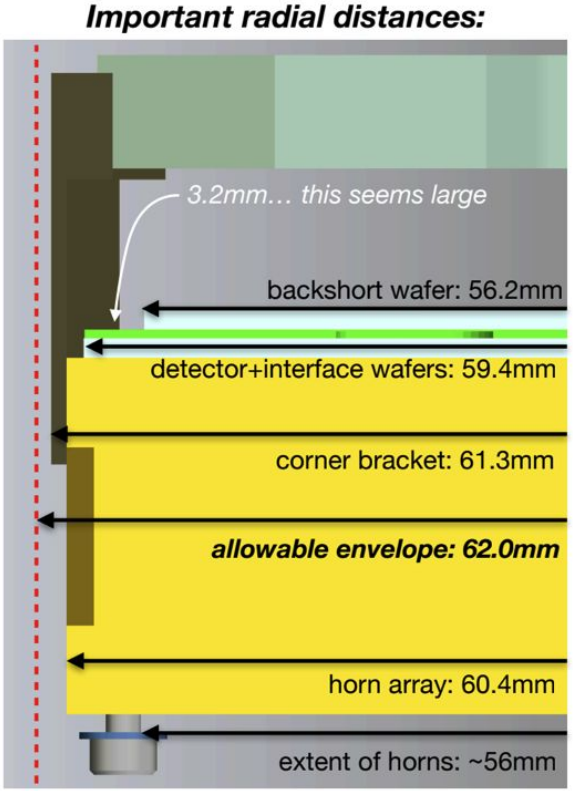
- Proposing a new v2 module design, enabled by higher density wiring on MUX Readout chip
- Helps several interface issues:
  - Readout box fit on back of module
  - Minimizes twisting and length of flex cables

See A. Anderson's MAT Parallel Talk

1) Module Design: SAT Interfaces

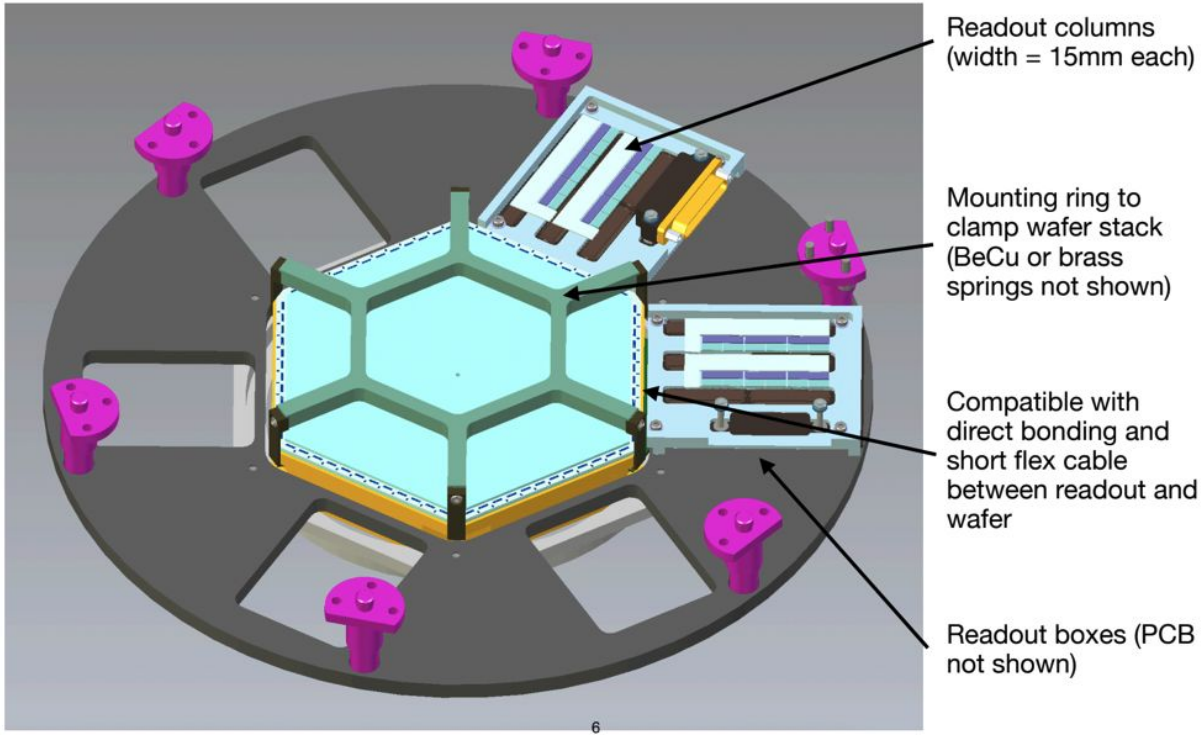
- See A. Anderson's MAT Parallel Talk
- WIth v2 design, the proposed SAT module layout fits better
- However, it is still tight, and will need to find ~2-mm from somewhere for module to fit.





1) Module Design: FY21 DRM R&D

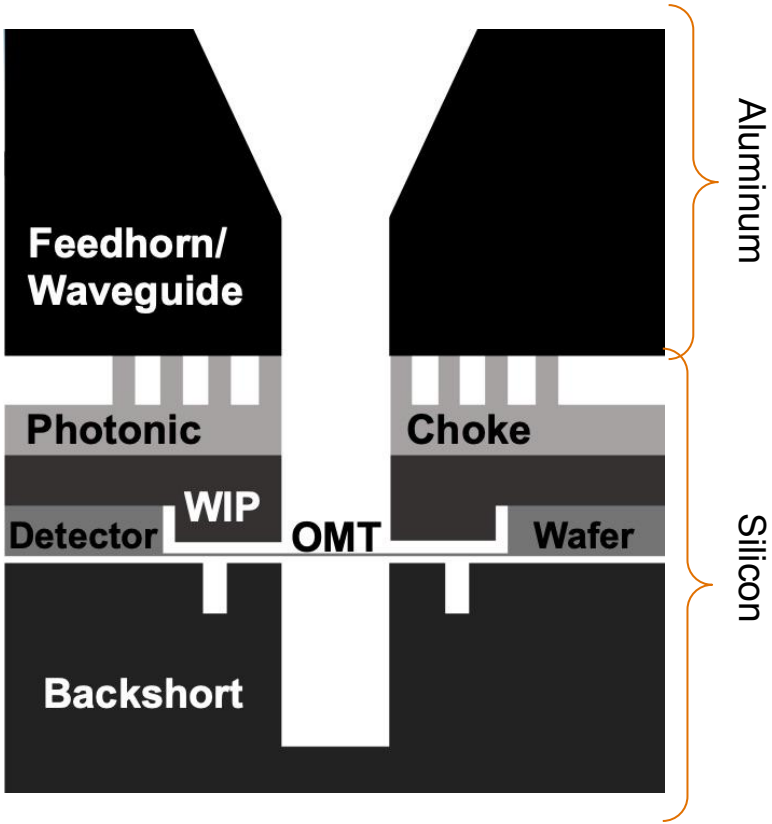
- FY21 DRM R&D plan calls for detector module testing of prototype detector wafers by Summer 2021
- Full detector and readout module design will not be ready on this schedule
- Designing intermediate detector and readout module that could still test ~700 detectors / wafer, and fit in baselined prototype DR testbeds



See A. Anderson's MAT Parallel Talk

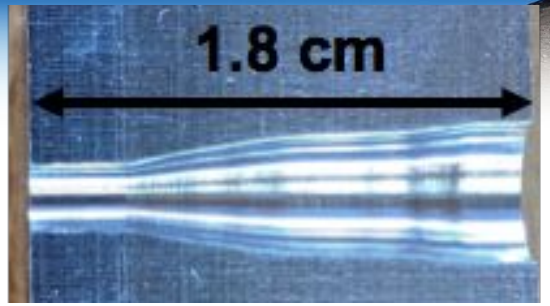
2) Horn Arrays and Interface Wafers

- Spline-profiled feedhorns made of (gold-plated) Aluminum 6061
- Silicon coupling “interface wafers” that sandwich detector wafer that form integrating cavity for OMT

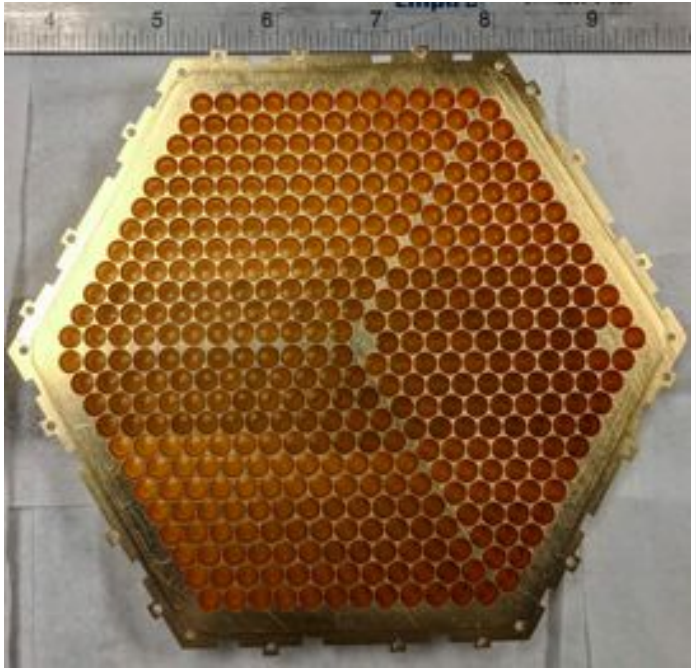


See S. Simon’’s MAT Parallel Talk

2) Horn Arrays



- Spline profiles optimized for performance requirements→ simulated estimates of systematic effects, efficiency
- **Final design requires set inputs:**
  - **Set pixel size**
  - **Defined waveguide cutoff and bands**
  - **Aperture stop angle**
  - **Any mechanical constraints (e.g. length)**
  - **Set input requirements**
- Will need to decide when inputs are frozen



See S. Simon's MAT Parallel Talk

2) Interface Wafers

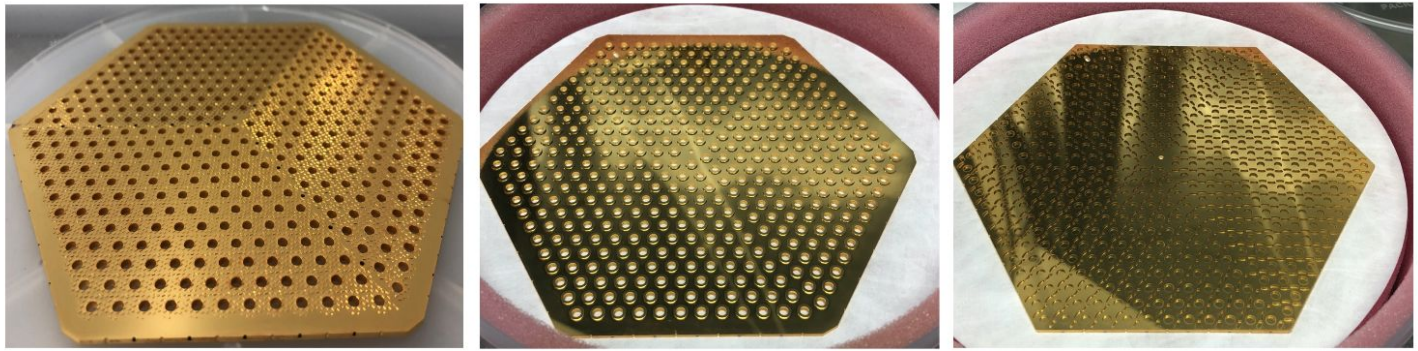


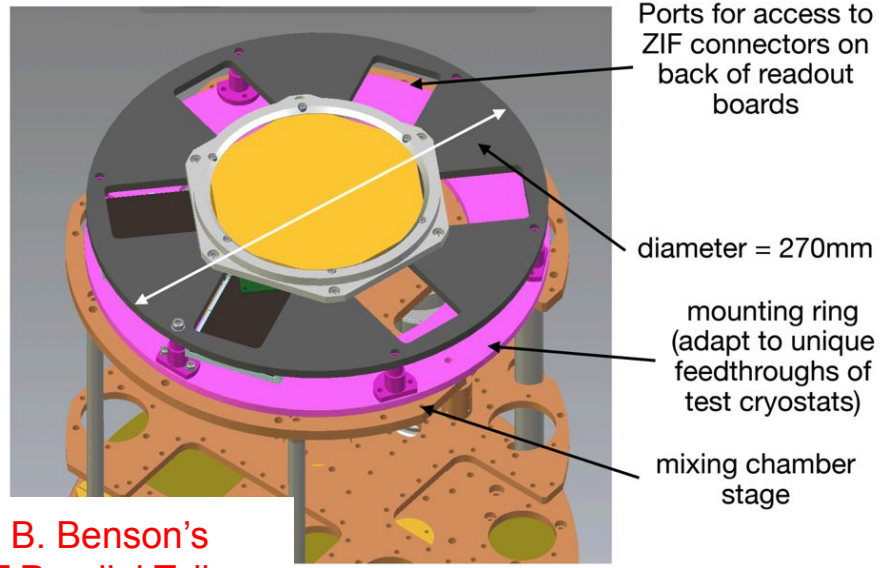
Figure 43: **Left:** A photonic choke wafer. **Center:** A waveguide interface plate. **Right:** A backshort array.

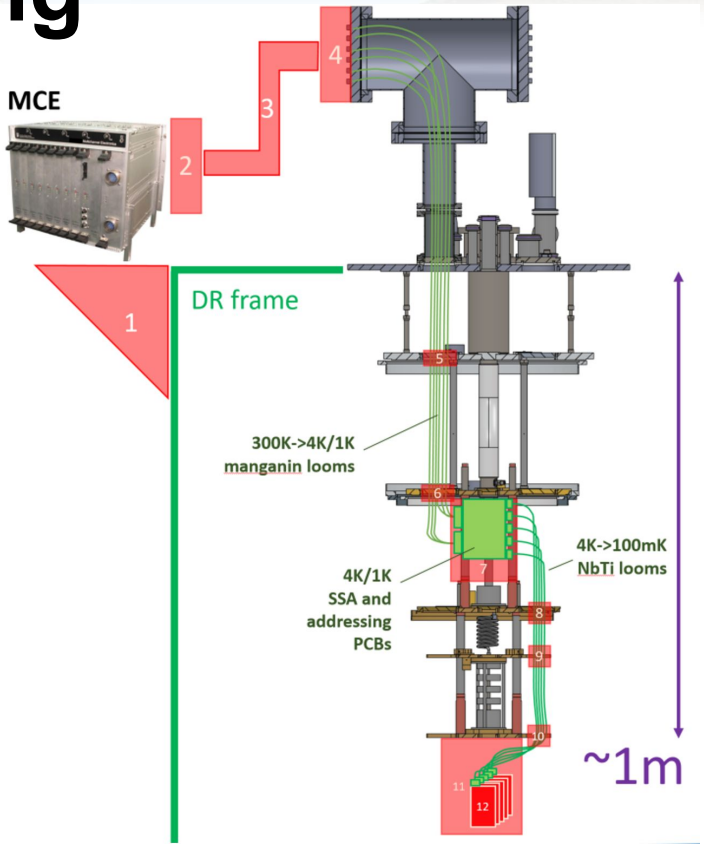
- NIST demonstrated process and design over past decade.
- For CMB-S4, need to seek alternative fabrication sites given number of wafers and cost.
- Early stages of writing RFI and discussions with potential vendors, both internal to S4 (SeeQC, SLAC) and commercial vendors

See S. Simon's Parallel Talk

3) Detector Module Testing

- For FY21 DRM R&D, working with readout on module design and readout chain to outfit 3x testbeds in collaboration for dark detector module testing.
- Expansion to new testbeds bottlenecked by having requisite TDM warm electronics in available DR cryostats





See B. Benson's MAT Parallel Talk

See G. Haller's Readout Parallel Talk

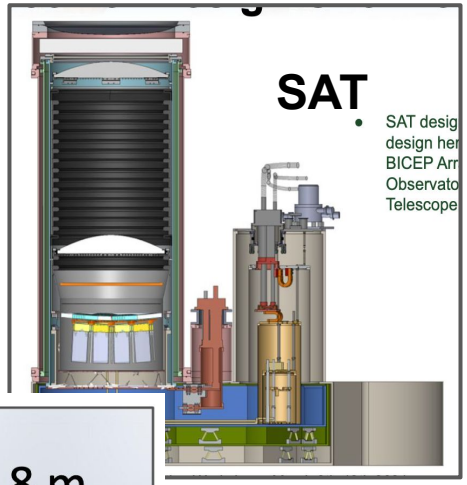
3) Detector Module Testing

nsition to new detector type

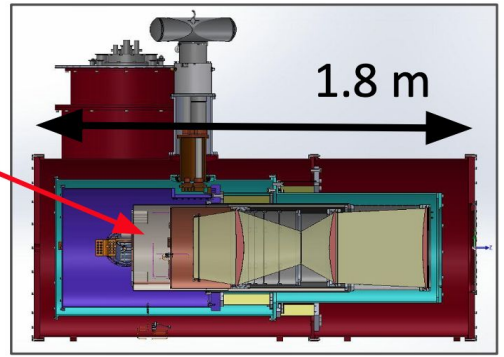
FY25A	FY25B	FY26A	FY26B	FY27A	FY27B	Total
10	10	10	8	10	10	86
14	16	16	16	12	6	106
16	16	16	16	4	4	102
10	12	14	16	16	14	108
8	12	16	11	11	10	68
4	4	4	4	4		33
62	70	76	71	57	44	503
104	117	127	119	95	74	841

MAT Req: Assemble and test ~600 detector modules over 3-year period

Production Test Cryostats: Shared design with LAT-CR or SAT single tube?



LAT-CR



Baseline Plan (from Agency Review):

- After CD-1, design and build 8x new CMB-S4 specific cryostats capable of testing ~6x detector wafers modules per cooldown, which will be spread over 2-3 testing sites.

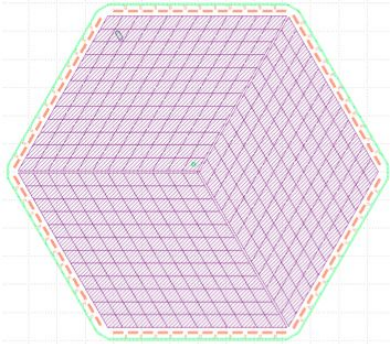
Summary/Conclusions

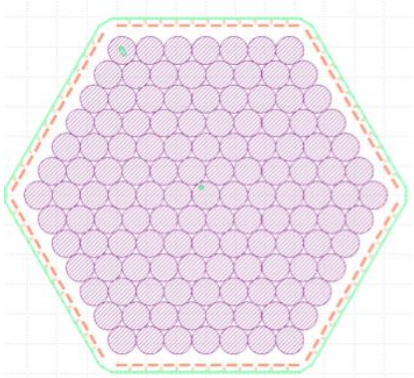
- Module design:
  - Making progress on prototype module design which is close to meeting requirements
  - FY21 DRM R&D will require intermediate design to match testing schedule
- Horn Arrays and Interface wafers.
  - Horn array production relatively straightforward, though detailed horn design will need inputs from SAT+LAT teams for detailed simulation & optimization.
  - Beginning RFI process for interface wafer production from fabrication sites, production will likely set schedule for early DRM optical testing.
- Detector Module Testing
  - Started outfitting 3x testbeds for DRM FY21 R&D testing, will expand to optical testing later in FY21 to match interface wafer and funding schedule.
  - New testbeds can be brought online with more warm readout electronics (See G. Haller's Readout Parallel talk)
  - Production testbeds will be designed after CD-1 to line up with FY25 production testing schedule.

Extras

CDFG RFI Summary

- Based on the detector parameters for LAT mid frequency bands (90/150)
- Two layouts: LAT MF (5.3mm pitch) and SAT-like MF (9.4mm pitch)
- Wafers will be assembled into modules
- Minimum goal: Dark tests
- Optical tests if possible (not in FY2021, maybe in CY21)
- Testing procedure included in RFI
- Changes since original RFI May 2020
  - Dec. 2020 High Tc Psat targets for the LATs were lowered (requires NDF for bare module tests, easier to fabricate)
  - Bondpad layout was changed from NIST (12 clumps of 25 pairs, 70micron pitch) to make it easier for bonding: 100 micron pitch
  - Frequency mapping to pads not specified; not important for CDFG tests, but critical for final layouts





90GHz	Parameter	Low	Target	High
Science TES	Psat (pW)	2.8	3.5	4.6
"	Tc (mK) *(at fixed Psat)*	139	160	184
"	$\frac{T_c^2 \ P_{sat}}{T_{c,0}^2 \ P_{sat,0}}$	-	1	1.32
"	Rn (mOhms)	8	12	16
High-Tc TES	Psat (pW)	26	29	(readout limit)
	Rn	2*Rn_science	2.5*Rn_science	-
	Tc	2.5*Tc_science	-	-

150GHz	Parameter	Low (pW)	Target (pW)	High (pW)
Science TES	Psat (pW)	6.0	7.5	9.9
"	Tc (mK) *(at fixed Psat)*	139	160	184
"	$\frac{T_c^2 \ P_{sat}}{T_{c,0}^2 \ P_{sat,0}}$	-	1	1.32
"	Rn (mOhms)	8	12	16
High-Tc TES	Psat (pW)	49	54	(readout limit)
	Rn	2*Rn_science	2.5*Rn_science	-
	Tc	2.5*Tc_science	-	-

Table 1: Deployment detector parameter targets and acceptable ranges.

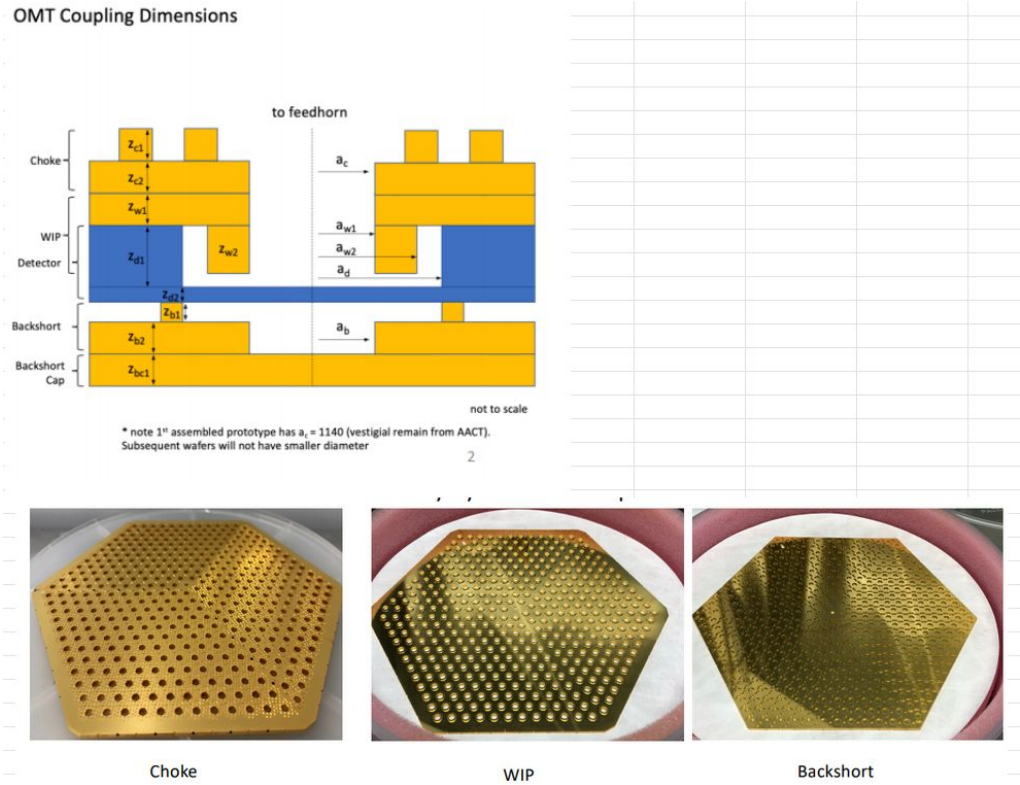
Recent challenges: Interface wafers

Interface/Coupling wafers: need to develop fabrication at multiple vendors (beyond NIST)

- Detector Fab sites interested
- RFI to go out soon
- Responses and available funding will impact schedule for optical tests
- Need to know detector layout to start fabrication

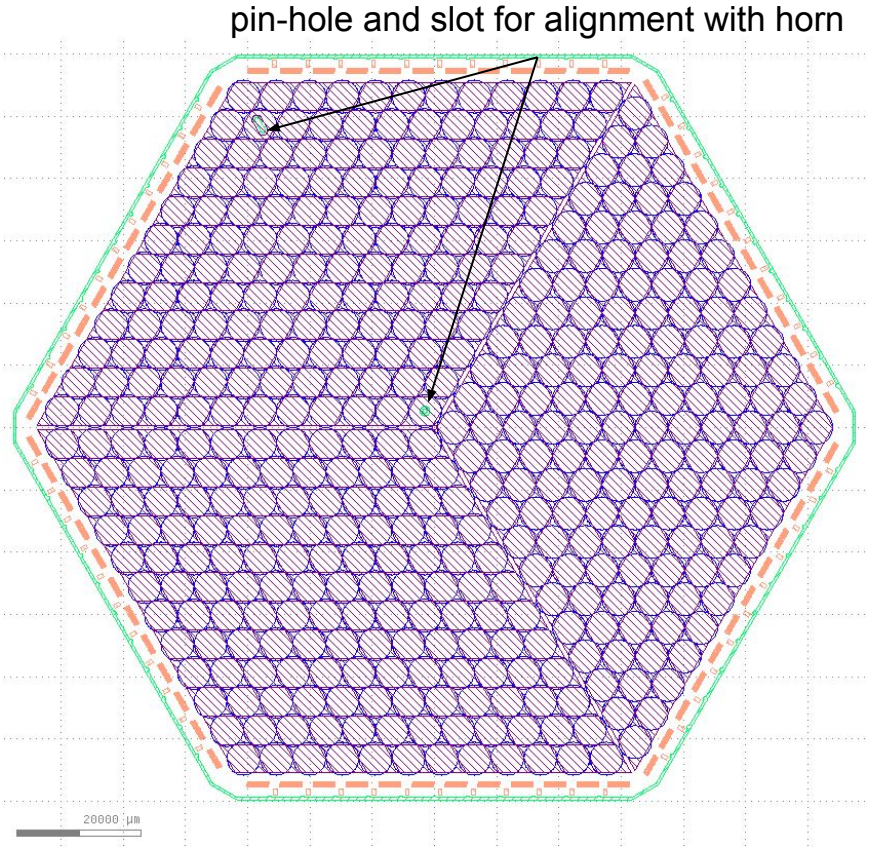
FY2021: Dark tests for CDFG wafers

Goal for CY2021: Optical tests



Module / Detector Interface

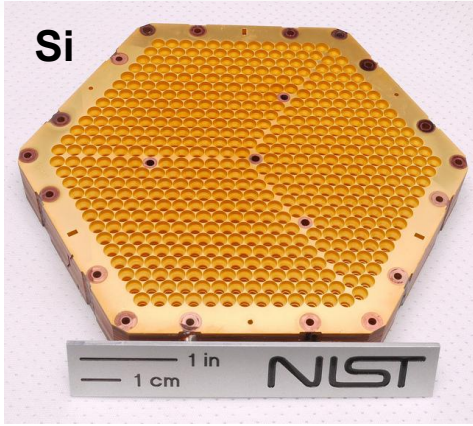
- Prototype S4 detector wafer design specification developed by CDFG + detectors WBS + module/test WBS (*CMBS4-doc-161-v6*)
- LAT (shown on right) and SAT 90/150 GHz designs satisfy pBD requirements
- Alignment with horns achieved with pin-and-slot to handle differential thermal contraction
- TES bondpads around perimeter
- Gold bondpads to improve heat-sinking around perimeter
- ***Based off SO design and experience***

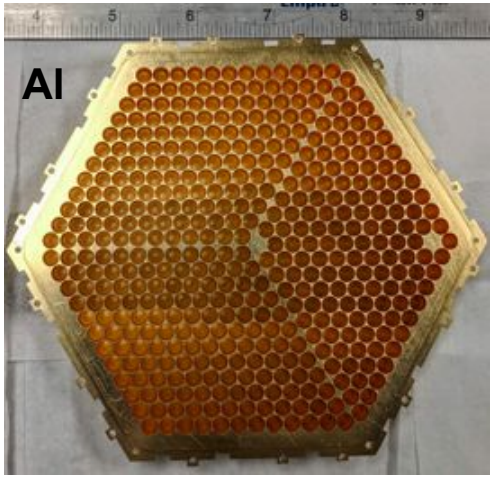


Credit: Anderson

Aluminum Feedhorns

- **Main modification for CMB-S4 is using Aluminum arrays**
- **Demonstrations**: BLAST-TNG, APEX-SZ, SPT-SZ - all used, aluminum feedhorn arrays coupled to MKIDs or TESes
- **SO**: Baselining Al feedhorn arrays with OMT coupling *(bottom)*
  - Enables enhanced RF and superconducting magnetic shielding with natural high pass filter from waveguide
  - Easier to assemble, good heat sinking, robust to thermal cycling
  - Mounting features can be machined into feed array
  - Alignment with pin + slot
  - **Fabrication status (January-2021):**
    - Beginning SO production MF (90/150 GHz) at U. Michigan shop.
      - Piggy-back fabrication of a set of CMB-S4 LAT MF and SAT MF arrays on top of this run.
    - SO prototype of UHF (220/280 GHz) beginning at U. Chicago shop.
    - Continue to explore alternate vendors for (larger-scale) production fab.

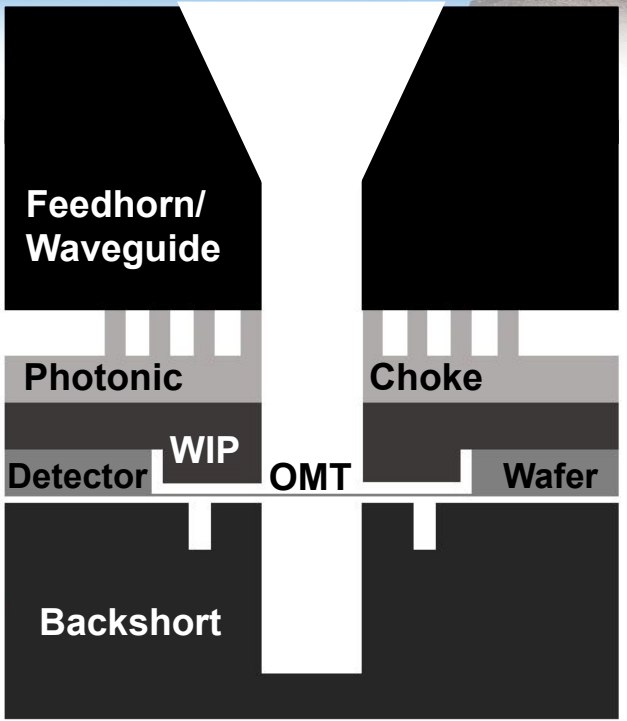


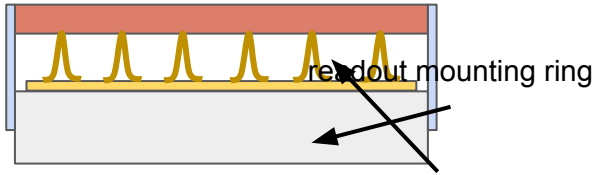


Credit: Simon

Interface Wafers

- Interfaces wafers: Includes the photonic choke, waveguide interface plate (WIP), and backshort wafer.
- Working with NIST on CMB-S4 MOA to share design, process steps, and potential procurement of interface wafers. Signed MOA is imminent.
- For FY21 R&D testing, will procure a set of three LAT MF interface wafers directly from NIST for tests this summer.
- FNAL (S. Simon) will work with NIST to explore commercializing interface wafer fabrication. Initial discussions with two vendors.





Credit: Simon