Detector Update
March Meeting

March 10, 2021

Brenna Flaugher, L2 Scientist (interim)
John Joseph CAM

CMB-S4

Presenter Background

Brenna Flaugher
Distinguished Scientist at Fermilab, Astrophysics Department Head

Previous experience
30 years of experience working on silicon detectors of various types
25 years experience in project management
Deputy Head of Fermilab Silicon Detector Facility
L2 manager for CDF Run IIB Silicon Vertex Detector
DES/DECam Project Manager
DESI Project Scientist and L2 Scientist for Integration and Commissioning

CMB-S4
2018-20 R&D Manager, Cost & Schedule development, Detector and Readout Task Force, Detector Fabrication Group, Governing Board and Speakers Committee member, CDFG
2020- present, Technical Integration Specialist, Interim L2 Scientist for Detectors, CDFG Chair

Outline

- Introduction
- Detector, Readout and Module (DRM) R&D plan
- Detector Fab plan
- Progress and Challenges
- Proposed steps beyond CDFG wafer delivery towards the FY22 detector pre-production plan

Introduction

Key Numbers and Parameters:

550,824 detectors on 503 hexagonal wafers, horn coupled, Dual Tc TESs

SAT wafers: 248 (now 216) , LAT wafers : 255 = 503 (now 471) science grade wafers

Plus ~12% overage and assuming ~67% yield: need to fabricate ~ 800 wafers

Eight different wafer types (assuming Pole and Chile LATs have same requirements)

Builds on strong heritage from Stage 2 and 3 experiments

Main challenge is scaling up production capacity - will need multiple fab. sites

Introduction

CMB-S4 Detector Fabrication Group (CDFG) established in Jan. 2020

- CDFG Charter doc-db 144: create a single, collaborative group to engage CMB-S4 detector experts during the design and fabrication phases of the CMB-S4 detectors. CDFG is an advisory group and meets weekly.

- CDFG Chair - BF (Interim Detector L2 scientist), Membership consists of representatives from ANL, JPL, LBNL-Seeqc, NIST, Stanford-SLAC, UCB (most are also L3 managers) and John Joseph (LBL, detector L2 CAM).

- CDFG Goals:
  1) address intellectual property and conflict of interest concerns
  2) fabricate prototype detectors which meet CMB-S4 acceptance criteria (CDFG-RFI)
  3) create single, coherent detector fabrication plan engaging multiple sites

Goal 1: Intellectual Property and Conflict of Interest

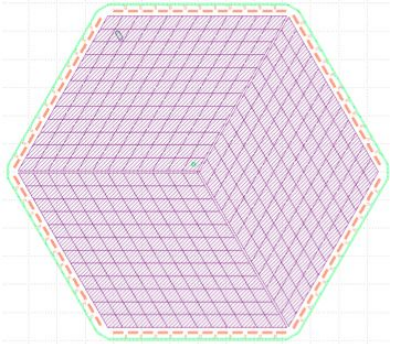
- CDFG developed draft agreement to address intellectual property and conflict of interest and delivered to LBL in Aug. 2020. (Detector Fab Review recommendation)
- LBNL Legal and NIST completed development of a Memorandum of Agreement (MOA) and IP management plan Jan. 2021.
- NIST has shared Detector and Horn Array designs for 90/150 GHz dichroic OMT coupled TES array and coupling parts (doc-db 634)
- Sharing of detailed technical information has been critical to making progress!

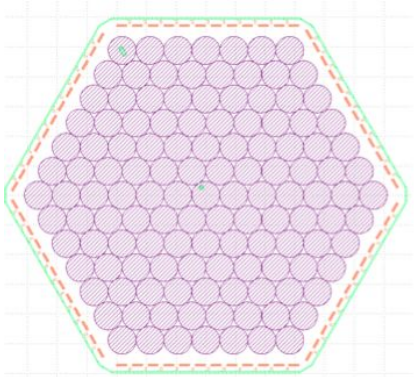
Goal 2) CDFG Prototype Development

- Organized a development plan with clear near-term detector wafer prototype specifications
  - 90/150 GHz, Horn-coupled
  - Plan series of dark/optical tests
  - Specified performance values, ranges for prototypes
- Solicited detector fabrication sites (via a “RFI”) to fabricate 1-2 prototype wafers per CMB-S4 specifications this year.
- Received 5 responses, recommendations for funding delivered to Project Director July 30, 2020
- Objectives
  - Demonstrate coordination of wafer fabrication of CMB-S4 prototype arrays at multiple sites
  - Provide wafers for early development of modules, readout and testing
  - Provide forum for open discussion, planning and communication of lessons learned
  - Develop CMB-S4 dual Tc TES capability at all potential fab sites

CDFG RFI Summary

- Based on the detector parameters for LAT mid frequency bands (90/150)
- Two layouts: LAT MF (5.3mm pitch) and SAT-like MF (9.4mm pitch)
- Wafers will be assembled into modules
- Minimum goal: Dark tests
- Optical tests if possible (not in FY2021, maybe in CY21)
- Testing procedure included in RFI
- Changes since original RFI May 2020
  - Dec. 2020 High Tc Psat targets for the LATs were lowered (requires NDF for bare module tests, easier to fabricate)
  - Bondpad layout was changed from NIST (12 clumps of 25 pairs, 70micron pitch) to make it easier for bonding: 100 micron pitch
  - Frequency mapping to pads not specified; not important for CDFG tests, but critical for final layouts





90GHz	Parameter	Low	Target	High
Science TES	Psat (pW)	2.8	3.5	4.6
"	Tc (mK) *(at fixed Psat)*	139	160	184
"	$\frac{T_c^2 \ P_{sat}}{T_{c,0}^2 \ P_{sat,0}}$	-	1	1.32
"	Rn (mOhms)	8	12	16
High-Tc TES	Psat (pW)	26	29	(readout limit)
	Rn	2*Rn_science	2.5*Rn_science	-
	Tc	2.5*Tc_science	-	-

150GHz	Parameter	Low (pW)	Target (pW)	High (pW)
Science TES	Psat (pW)	6.0	7.5	9.9
"	Tc (mK) *(at fixed Psat)*	139	160	184
"	$\frac{T_c^2 \ P_{sat}}{T_{c,0}^2 \ P_{sat,0}}$	-	1	1.32
"	Rn (mOhms)	8	12	16
High-Tc TES	Psat (pW)	49	54	(readout limit)
	Rn	2*Rn_science	2.5*Rn_science	-
	Tc	2.5*Tc_science	-	-

Table 1: Deployment detector parameter targets and acceptable ranges.

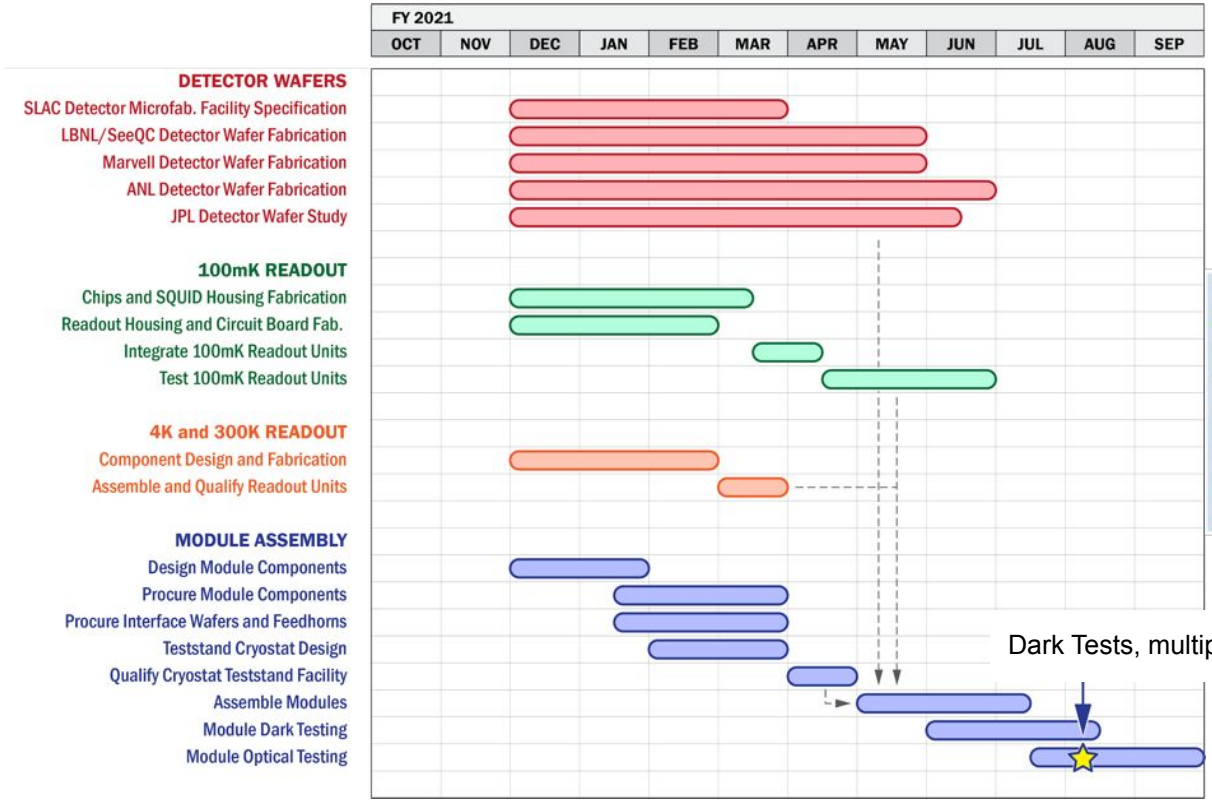
Developed FY21 DRM R&D plan to fit in available funding

- **Detectors:** Fabricate CDFG RFI wafers at ANL, Seeqc and UCB/Marvel, use minimal and/or existing on-site testing equipment (DC-Squid, resistance bridge)

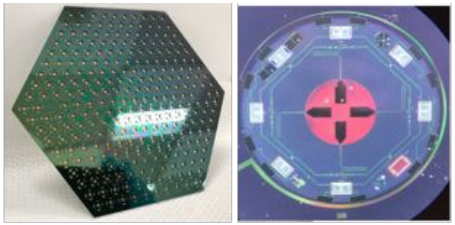
- **Readout:** design/fabricate 3 100mk modules to read out ~100 channels each, cables and 4K components for 3 test sites

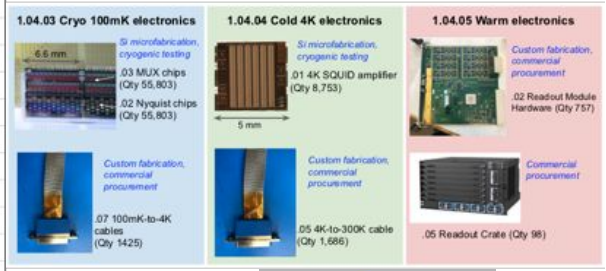
- **Modules and testing:** Design/fabricate parts for 3 modules, use existing/borrowed cryostats and MCE crates.
  Identified 3 testing sites: FNAL, SLAC dark and optical, Univ. Illinois Urbana Champaign (UIUC) dark tests

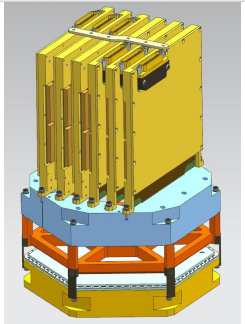
DRM FY21 R&D Schedule Overview



Dark Tests, multiple sites







CMB-S4

Goal 3: Detector Fabrication Plan

Assumptions:

- Group wafers by number of pixels and frequencies, switching between similar frequencies and number of pixels is easier than big changes
- Start with the types we need most (MF)
- Initially use all 6 sites, minimize need to hire/train new people and procure new equipment.
- Potential downselect to fewer sites based on performance, cost and schedule
- Module assembly, Testing and RO can keep up with Detector fab (TBD- stay below 250 modules/year)
- Potential fab sites to demonstrate capability to produce CMB-S4 wafers in FY22.
- CDFG RFI wafers (FY21) are 1st step.

Pixels/ wafer		Number Wafers	name
12	SAT 30/40GHz	28	SAT LF
27	LAT 20GHz	4	LAT ULF
48	LAT 30/40GHz	25	LAT LF
147	SAT 85/145, 95/155	168	SAT MF1, MF2
432	LAT 90/150	162	LAT MF
432	LAT 225/278	64	LAT HF
469	SAT 220/280	52	SAT HF
		503	

Detector Fabrication Plan cont.

- Each detector type will be fabricated by at least 2 sites
- Build on existing experience (NIST - SO, LAT MF, JPL - SATs, LBL and UCB support each other, SLAC will start production in FY25, etc)
- Assignment of detector types to fab sites allows focused R&D

Pixels/ wafer		Number Wafers
12	SAT 30/40GHz	28
27	LAT 20GHz	4
48	LAT 30/40GHz	25
147	SAT 85/145, 95/155	168
432	LAT 90/150	162
432	LAT HF	64
469	SAT 220/280	52
		503

Site 1 = ANL	Site 2 = JPL	Site 3 = SEEQC	Site 4 = NIST	Site 5 = SLAC	Site 6 = Marvell
	6	10			12
					4
		8			17
	84	84			
66			64	32	
20			44		
	16			36	
86	**106**	**102**	**108**	**68**	**33**

Detector Fabrication Plan Assumptions

- It is preferable to finish off detectors in integral units of cryostats (SAT and LAT)
  - integration and testing in the US
  - deployment after testing fully loaded cryostats
  - Preproduction modules could be used for some tests
- Plan (next page)
  - 1st SAT finished in FY24
  - SPLATR finished in first half of FY25
  - Assumes “sufficient” funding
- Many other distributions possible, this is just a start

Wafer type	Total Science Wafers	number per tube or cryostat
SAT 30/40GHz	28	14
SAT 85/145, 95/	168	28
SAT 220/280	52	13
SPLATR		
LAT 20GHz	4	4
LAT 30/40GHz	9	9
LAT 90/150	54	54
LAT HF	18	18
CHLATR		
LAT 30/40GHz	16	8
LAT 90/150	108	54
LAT HF	46	23

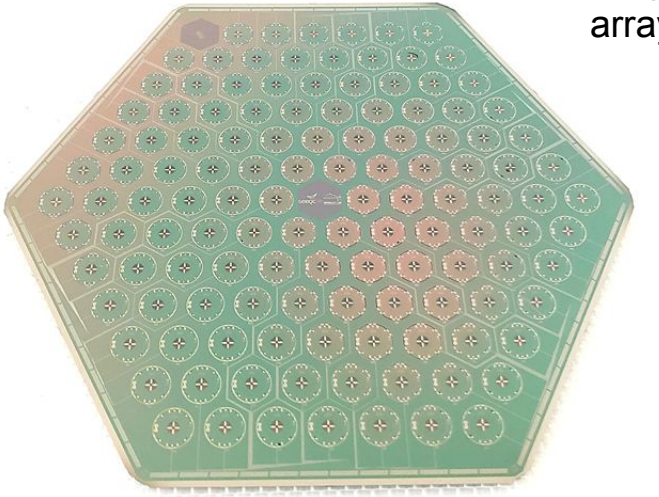
Draft Production Fabrication plan (v5)

- Rates and detector types discussed with each site and iterated.
- Production rates require minimum ramp-up in capabilities at all sites
- Additional capacity is possible at most sites, with appropriate warning
- Plan to reoptimize based on performance, cost and schedule at least annually

PRODUCTION		Split years into part A and B for transition to new detector type									
	FY23A	FY23B	FY24A	FY24B	FY25A	FY25B	FY26A	FY26B	FY27A	FY27B	Total
Site 1 = ANL	2	8	8	10	10	10	10	8	10	10	86
Site 2 = JPL	2	8	8	8	14	16	16	16	12	6	106
Site 3 = SEEQC	2	8	10	10	16	16	16	16	4	4	102
Site 4 = NIST	2	8	8	8	10	12	14	16	16	14	108
Site 5 = SLAC					8	12	16	11	11	10	68
Site 6 = Marvell	1	3	4	5	4	4	4	4	4		33
Total Science Grade	9	35	38	41	62	70	76	71	57	44	503
~ Number of wafer modules to test (inc. 12% overage and 67% yield)	15	59	64	69	104	117	127	119	95	74	841

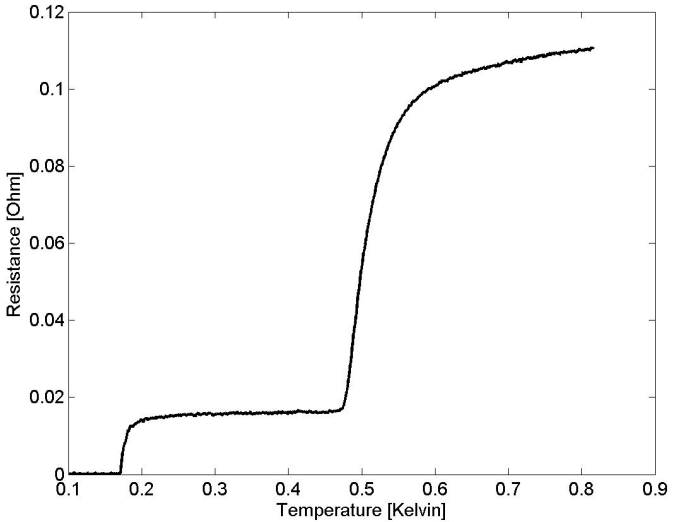
Recent Progress

Seeqc has delivered single Tc CDFG wafer to LBL for testing. Fabrication of dual Tc wafer was completed this week.



Single Tc TES
array from Seeqc

Dual Tc TES
demo from Seeqc



Recent Progress

UCB-Marvel is making progress on single Tc wafer (same layout as Seeqc):

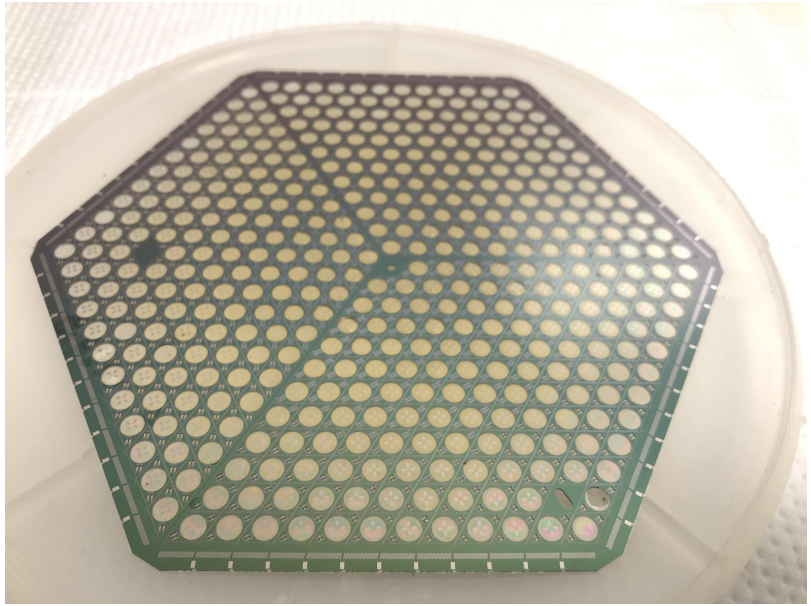
Photographs of the CDFG wafer being fabricated at UC Berkeley for CMB-S4. (a) A photograph of the wafer with most of the front side processing complete. (b) The OMT membrane and slots for the coplanar waveguide coated with the niobium OMT probes and microstrip lines. These elements will be released at SeeQC using backside DRIE. (c) The 25x200um TES and Ti load resistor shown at the center 150 GHz 'Top' bolometer island. A portion of the SAT-MF 90/150 GHz diplexer is shown in the bottom right.

Recent Progress

Argonne:

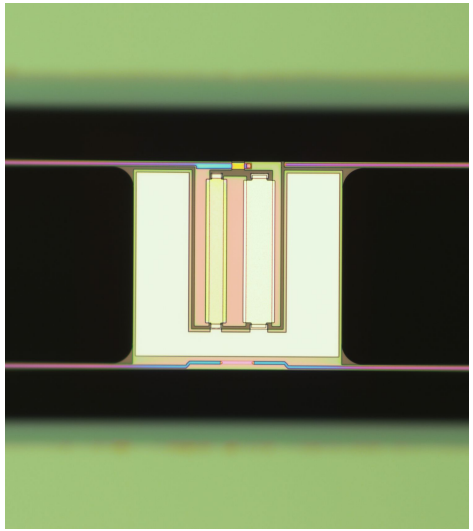
Sept 2020: tested OMT coupled array with TES science transitions at CDFG goal for Rn, Tc, Psats, and the dual Tc test structures with transitions at ~160 mK and ~400 mK.

March 2021: completed a couple wiring layer wafers (on path for CDFG wafer). Will be delivered to Fermilab next week for module interface checks.

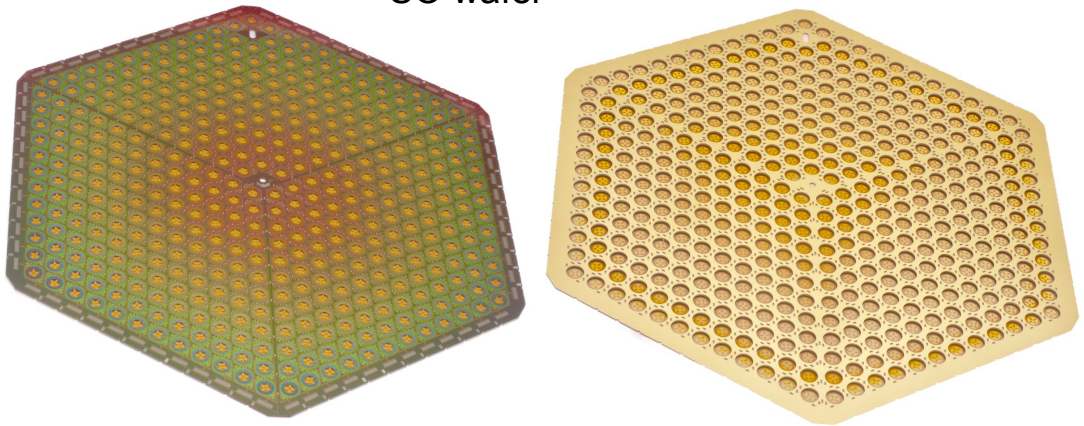


Recent Progress

NIST is making progress on Dual Tc development, SO layout matches LAT MF, (except for dual Tc TES and bondpad locations)



SO wafer

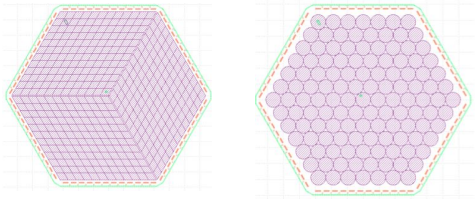


Recent challenges: Matching wafer layouts to Fab. site expertise

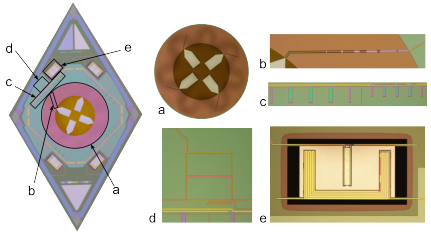
Fab sites have different equipment, experience and expertise

- Hex vs Rhombus layout
  - All sites could make Hex wafers (or square or rectangle)
  - Rhombus layout requires x3 more masks and lithography steps and stitching if sites do not have a stepper that can rotate
  - NIST, SLAC have equipment to do Rhombus, ANL is doing R&D for Rhombus layout with their existing equipment
  - LBL/Seeqc, Marvel and JPL prefer no crossovers and Hex layout
- Wiring Crossover/under and Mapping Freq. to bond pads:
  - Hex: bondpad pairs alternate frequencies, does not require crossovers: see Toki's talk (slide)
  - Rhombus: one freq per side, layout as implemented by NIST has lots of crossovers: see Shannon's talk (slides)
- RF structures internal to the pixel differ
  - Will need to document what was included in RF simulations (2D or 3D, coupling and horns) and what has been demonstrated for upcoming reviews
  - Size matters - some features may be too large for dense layouts
- Discussed with DSAC: supported allowing mix of approaches based on fab. site experience, but don't mix Hex and Rhombus in same wafer types. Different layouts for different bands seems fine.

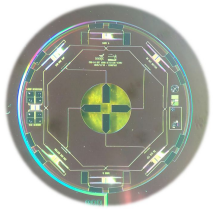
CDFG wafer layouts



NIST



LBL (Seeqc and UCB)



Recent challenges: pBD has all Rhombus (except SAT HF), this is not well matched to Fab. site expertise

We don't have time or funding to do the R&D required to have all sites do the same things.

The balance between hex and rhombus wafers in the pBD is not well matched to current capabilities of the fab sites.

More hex layouts would improve flexibility to optimize based on cost, schedule, demonstrated yield and risk - This is really critical as the project moves forward

What are the impacts of shifting some of the wafer designs from Rhombu to Hex?

Proposed Path forward (will be discussed in detector parallel session):

1) Develop Hex layouts for all wafers to see what actually fits considering site dependent active area, alignment pin/slot and room for darks, horn diameter, wire routing to bondpads
2) Present flowdown team with options based on these layouts and encourage investigation into a switch to Hex
3) Need to resolve reasonably soon: implications for module design, optical design could be large

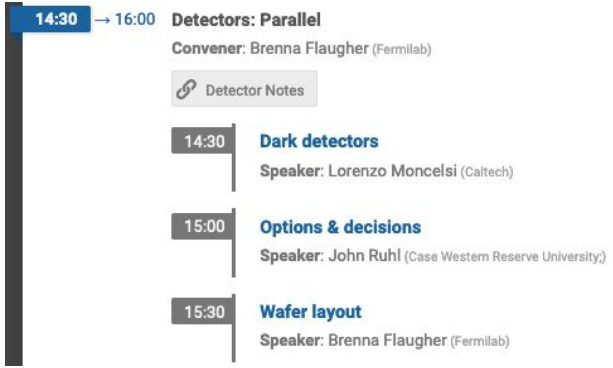
NOTE: Here "Horn diameter" means pixel pitch vs. the horn aperture size, which will include some sidewall thickness

Rhombus layout pixel count possibilities				
Number of Rings	Pixels/wafer	Horn diameter (mm)	Horn diameter (mm)	Used in
Active wafer area diameter		130.00	134.00	
2	12	30.20	31.10	SAT 30/40GHz
3	27	20.70	21.10	LAT 20GHz
4	48	15.70	16.10	LAT 30/40GHz
5	75	12.70	13.0	
6	108	10.60	10.90	
7	147	9.10	9.40	SAT 85/145, 95/155
8	192	8.00	8.20	
9	243	7.10	7.30	
10	300	6.40	6.60	
11	363	5.80	6.0	
12	432	5.30	5.50	LAT 90/150, 220/280
13	507	4.95	5.10	
14	588	4.60	4.70	
15	675	4.30	4.40	
16	768	4.00	4.15	
17	867	3.80	3.90	
18	972	3.60	3.70	
19	1083	3.40	3.50	
20	1200	3.20	3.30	
21	1323	3.05	3.15	

HCP layout pixel count possibilities					
Pixels on side of hex	Pixels across diameter	Pixels/wafer	Horn diameter (mm)	Horn diameter (mm)	Used in
			130.00	134.00	
1	1	1	130.00	134.00	
2	3	7	43.33	44.67	
3	5	19	26.00	26.80	
4	7	37	18.57	19.14	
5	9	61	14.44	14.89	
6	11	91	11.82	12.18	
7	13	127	10.00	10.31	
8	15	169	8.67	8.93	
9	17	217	7.65	7.88	
10	19	271	6.84	7.05	
11	21	331	6.19	6.38	
12	23	397	5.65	5.83	
13	25	469	5.20	5.36	SAT 220/280
14	27	547	4.81	4.96	
15	29	631	4.48	4.62	
16	31	721	4.19	4.32	
17	33	817	3.94	4.06	
18	35	919	3.71	3.83	
19	37	1027	3.51	3.62	
20	39	1141	3.33	3.44	

FY22 R&D and pre-production

- Focus for post-CDFG wafers and pre-production is to produce wafers that, if successful, could be deployable
- We need to resolve a few issues before we can make production layouts (will be discussed in parallel sessions):
  - Number of darks (and what are they)
  - Hex vs rhombus
  - Internal pixel layouts (documentation)
  - Bondpad locations, materials and frequency mapping
  - RF coupling design and interfaces to detectors
  - Readout and module design and interfaces
- Preproduction
  - Design fab cycle takes 3 months
  - 2 preproduction cycles (6 months total) needed to make 4 near science grade wafers
  - Each site will focus on 1 or 2 detector types
  - Decision on 2nd type will depend on funding and success with 1st type



Preproduction	FY22A	FY22B
Site 1 = ANL	LAT MF	LAT MF
Site 2 = JPL	SAT MF	SAT HF
Site 3 = SEEQC	SAT MF	SAT LF
Site 4 = NIST	LAT MF	LAT HF
Site 5 = SLAC		
Site 6 = Marvell	SAT LF	LAT LF

Summary/Conclusions

- Funding is very limited, but all fab sites are engaged in technical discussions and planning (CDFG and R&D meetings)
- Early R&D funding, leveraged by LDRD, ECRP and SBIR funds, has made great progress:
  - Wafers with OMTs have been fabricated by ANL and LBNL/Seeqc
  - Dual Tc wafer (ANL) and test structures (Seeqc) show encouraging performance
  - ANL, Seeqc, Marvel are on track to deliver CDFG wafers in a few months (~ May)
- Overall DRM R&D plan, while funding limited, is on track to fabricate and test early prototype CMB-S4 modules with the CDFG wafers in FY21
- Development of a CMB-S4 detector wafer production plan is in progress, more flexibility on wafer layouts is needed to allow for future optimization of cost and schedule
- Detector parallel will address issues that must be resolved before we can make CMB-S4 wafer layouts: Hex vs Rhombus, Darks, and many detailed detector requirements
- Overarching goal is to start pre-production wafer fabrication FY22.

Extras

Recent challenges: bondpad to detector mapping- resolved except for Darks

The push to settling on the design of CMB-S4 MF wafers uncovered an undefined issue wrt how the frequency bands are routed to the bond pads:

- LAT MF - tied to NIST design of SO wafers: Rhombus, 90 and 150 bands go to different sides, has crossovers on the wafer to separate the bands. Shannon gave a nice summary at a CDFG meeting (slides)
- SAT-like CDFG wafer - Hex layout with bond pads alternating frequencies, no crossovers on the wafers. Toki's summary of Hex options (also from CDFG meeting) (slide)
- **RO has determined that they can accommodate these two different mappings** of frequencies to bondpads, and the highest density (SAT HF 469 pixels) wafer layouts
- **We need guidance on number and detailed definition/use cases of Darks (Lorenzo collecting information for presentation in the Det. parallel)**

Recent challenges: Interface wafers

Interface/Coupling wafers: need to develop fabrication at multiple vendors (beyond NIST)

- Detector Fab sites interested
- RFI to go out soon
- Responses and available funding will impact schedule for optical tests
- Need to know detector layout to start fabrication

FY2021: Dark tests for CDFG wafers

Goal for CY2021: Optical tests