Report Back - Readout

Tucker Elleflot for Readout Working Group
Convener: Ed Young
Note taker: Riccardo Gualtieri

March 10, 2021

Outline

Summarizing presentations:

- **Prototype design status:** Gunther Haller
- **Magnetic Shielding:** Alessandro Schillaci, Lorenzo Moncelsi
- **SAA location (4 K vs 1 K):** Darcy Barron
- **Warm Electronics:** Gunther Haller

Along with discussion from many others during readout parallel session

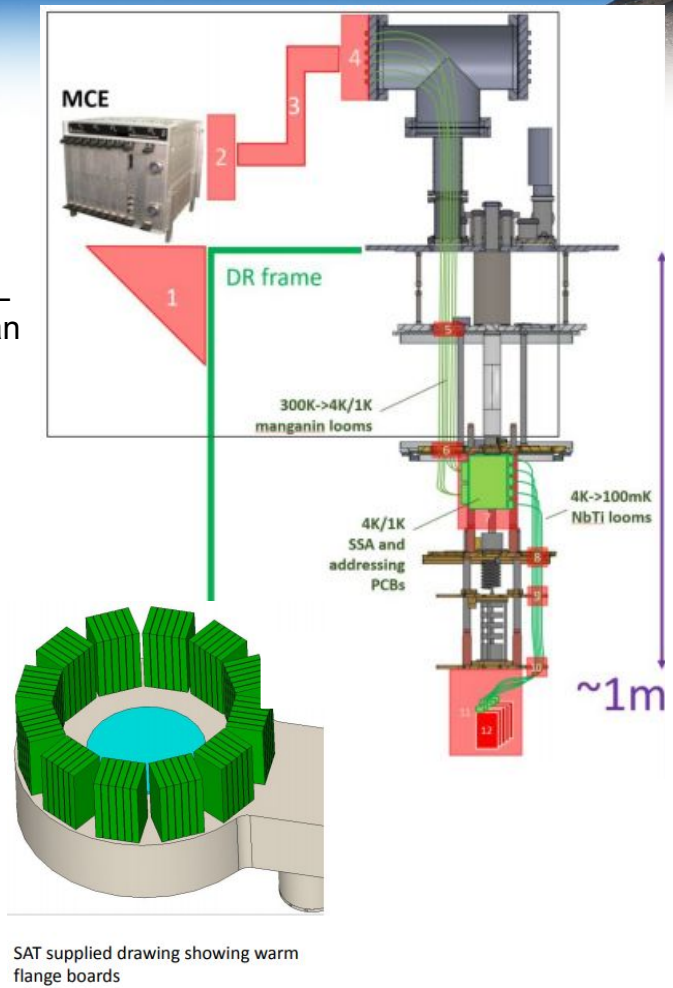
Readout Status for CDFG Testing
Gunther Haller

Warm Electronics

- MCE is obsolete, but have several for CDFG wafer testing at SLAC, UIUC, FNAL
  - Limited testing capabilities (41 row readout, 1-2 sides of a wafer only). Can use for CDFG testing
- New readout boards (replacing MCE)
  - Need project funds for fabrication, testing, software development
  - Mount directly to cryostat, no warm cable
  - Backward compatible with MCE
  - Liquid cooling (define requirements and coordinate with other working groups)
- Cable and RF shield between cryostat flange and MCE
  - Vacuum flange ordered
  - RF shield design started
  - Cable designed, quote received, about to order

Cryogenic Cables

- Connectors ordered
- Quote for cables received from Tekdata



SAT supplied drawing showing warm flange boards

Readout Status for CDFG Testing

Gunther Haller

4 K SAA Module

- Schematic complete and reviewed, layout started
- Mechanical enclosure design when FY21 funds arrive

100 mK Row Address Module

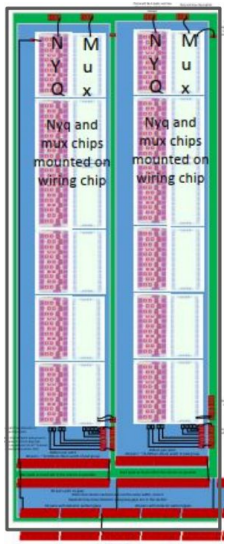
- Schematic complete

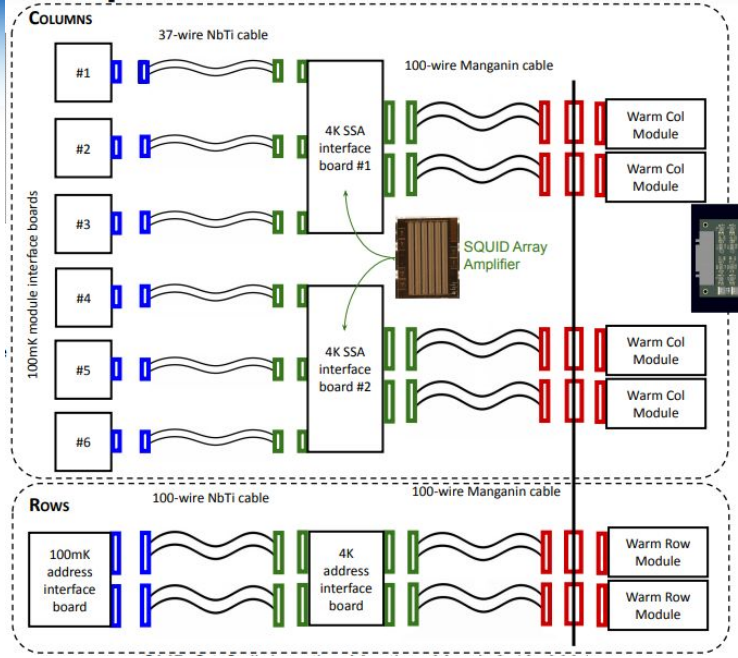
100 mK Column Readout Module

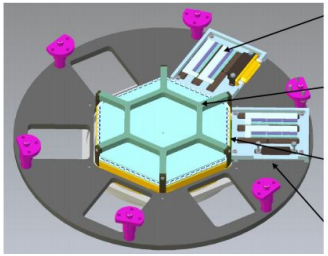
- Superconducting signal connections
  - Several options, further study required
- Two column prototype for CDFG wafers
  - Silicon chip with superconducting traces
  - Readout: 19 pixels/side for LBNL CDFG wafer and 29 pixels/side for ANL CDFG wafer

Nyquist Chips

- Can accommodate alternating TES frequencies as well as one frequency/detector side with Nyquist chip that has two TES bias lines
  - Previously demonstrated by NIST







A. Anderson, B. Benson, G. Derylo,

Planar readout configuration for CDFG testing (NOT observation)

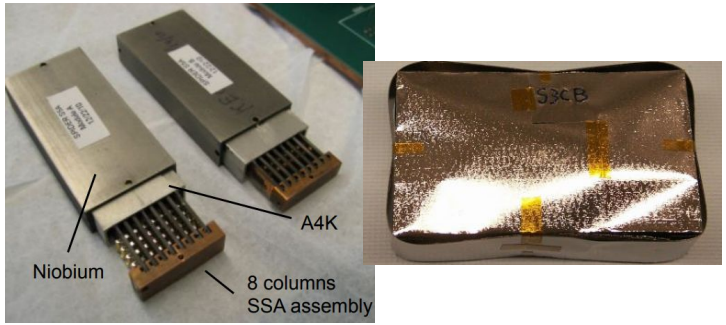
Magnetic Shielding - A. Schillaci, L. Moncelsi

Outer A4K shield at 50 K or 4 K is crucial to performance
Aim to minimize magnetic flux density at location of SQUIDs

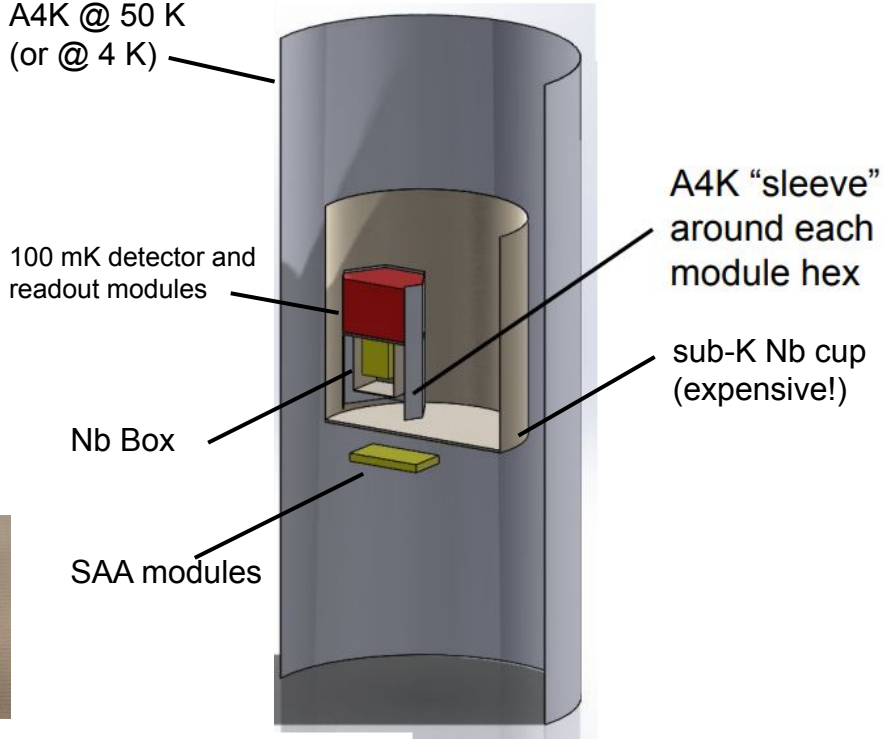
Lots of options to mitigate magnetic fields, some may be required in SAT/LAT

Input requested from Flowdown to help define shielding requirement

Note: SAA shielding previously done with Nb and A4K shield along with 10x layer Meglas wrap



One possible toy scheme to model/simulate



1 K vs 4 K SAAs - Darcy Barron

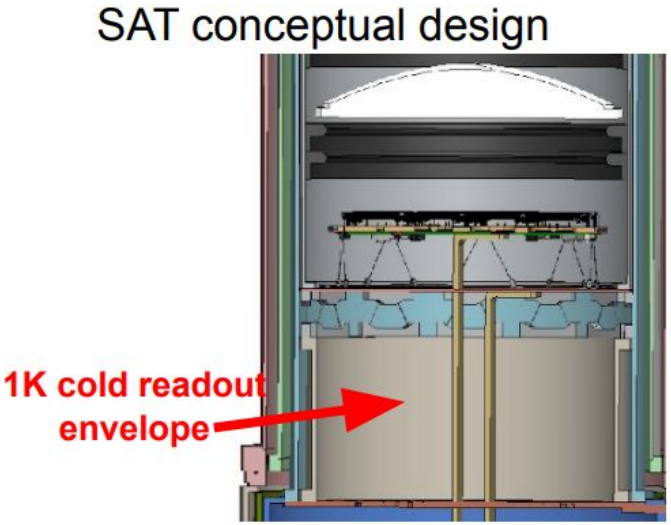
At this stage, no obviously strong readout driver for location of SAAs (still checking readout constraints)

Some advantages to putting them at 1 K stage:

- Much more margin on temperature (must be < 5 K)
- Easier to make RF clean space that includes SAAs
- Potential for better magnetic shielding of SAAs

Further studies:

- Cryogenic budget: some uncertainty in SAA power dissipation
- Cable length requirements (SQ1 to SAA, SAA to warm)
- Space constraints in LAT
- Any differences in requirements for fab and screening for 1K vs 4K



Interfaces

- Funds needed for
  - Development of new warm readout boards
  - Design of 4 K SAA mechanical enclosure
- Liquid cooling of warm readout boards
  - Readout to define requirements and interface with other groups
- Magnetic shielding
  - Important input to SAT and LAT designs
  - Need to understand shielding requirement better from Flowdown
- SAA location
  - Need to interface with SAT and LAT to determine more realistic wire lengths and cryogenic loading
  - Space constraints in LAT