Readout Preliminary Baseline Design Overview

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Plenary Session, Tuesday, March 9, 2021
Outline

- Readout Function and Scope
- Driving Requirements
- Architecture: Time-division multiplexing
- CMB-S4 implementation
- Design highlights
  - 100mK
  - 4K
  - 300K
- Optimization
- Workflow: Production/Screening/QA
Readout Functions and Scope

Functions:
1. Bias the Transition-Edge Sensor (TES) bolometers on their silicon wafers
2. Amplify measured signals
3. Sample/Digitize/Filter and hand off timestream to DAQ

Scope:
All the hardware and software elements that integrate/interface with the Modules, LAT, SAT and DAQ to provide above readout functionality
## Driving Requirements

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<tr>
<th>Requirement</th>
<th>Trace</th>
<th>Value</th>
<th>Origin</th>
<th>Validation</th>
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| Supply electrical bias power appropriate to the TESs                       | MR 2.0, 3.0       | Exact values are optimized for each observing frequency and telescope. | Flowdown from sensitivity requirements in each band.                                                                        | 1. Verify warm electronics DAC performance meets specifications.  
2. Verify TES operation (with expected saturation powers) using prototype system.                                  |
| Channel operability in operating instrument (readout-only)                  | MR 1.1, 1.2, 2.0, 3.0, 4.0 | >=95%                                                               | Flowdown from total instrument sensitivity requirements.                                                                   | 1. Screen components with interconnects.  
2. Demonstration during prototyping that screening achieves yield requirement.                                           |
| Noise equivalent current of readout at TES bolometer                       | MR 1.1, 1.2       | <5% increase in total white noise level due to readout. 1/f shape & level TBD. | Flowdown from science requirements.                                                                                        | Measure noise power spectrum of integrated prototype readout system both open & with TES bolometers.                         |
| Crosstalk                                                                  | MR 1.1, 1.2, 2.0  | TBD from flowdown simulations.                                       | Systematic error budget from instrument modeling and flowdown.                                                              | 1. Measure inductor coupling in MUX chips (expected to be dominant) in prototypes.  
2. Measure crosstalk in individual components.  
String test measurement in prototype system (no TESs).                                                                 |
| Systematic error budget from instrument modeling and flowdown.             |                   |                                                                    |                                                                                                                                |                                                                                                                                 |

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Architecture: Time-division multiplexing

- Arrange TESes of a detector wafer as a 2D logical grid
- Read one “row” at a time; switch at ~10s of kHz
- Connections to 300K scale as perimeter, not as area
- CMB-S4 will use ~64 “rows” (MUX64)

Uses *Superconducting Quantum Interference Devices* (SQUIDs) as cryogenic first- and second-stage amplifiers and as row switches. Microfabricated on silicon with superconducting materials.

Room temperature electronics are simple, low-frequency boards with low-noise precision ADCs and DACs

**TDM is a mature technology with heritage from Stage-2 and Stage-3 CMB experiments**
CMB-S4 implementation (1)

- Support up to 1920 TES readout per wafer
  - 1920 TES = 320 TES x 6 edges
  - Practical limit ~1872 TES (bonding interface)
- One 100mK RO unit for each wafer edge
  - 320 TES = 5 columns x 64 rows
  - 64 rows built using 6x 11-channel TDM SQUID multiplexer chips (6 usable for darks, diagnostics)
- 64 Row Addressing
  - 64 row switches operated per module by row addressing pairs from 300K to 100mK, daisy chained through 100mK RO units
- 5 Column Readout
  - 5 columns’ TES biases, SQUID bias and feedback carried from 300K to 100mK
  - SQUID Array Amplifier per column at 1K or 4K

6x 100mK RO units attached to detector module. Each can service 300 TES in 64 row x 5 column configuration. In development.
CMB-S4 implementation (2)

**Columns**

- 100mK module interface boards
- 4K SSA interface board #1
- 4K SSA interface board #2
- SQUID Array Amplifier
- Warm Col Module
- Warm Col Module
- Warm Col Module
- Warm Col Module
- Warm Col Module

**Rows**

- 100mK address interface board
- 4K address interface board
- Warm Row Module
- Warm Row Module

**Cable Types**

- 37-wire NbTi cable
- 100-wire Manganin cable
- 100-wire NbTi cable
- 100-wire Manganin cable

**Other Components**

- 100mK Readout units on Detector module
- SQUID multiplexer and TES bias chips
- Warm electronics modules
- Cryogenic cabling

**Legend**

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100mK: Technical Design (1)

100mK Readout Units
- One per detector hex edge
  - 5 columns x 64 rows
- Route signals between detector wafers, 100mK silicon, cabling to 4K
- Provide mechanical support and heat-sinking for 100mK cryo silicon
- Shield 100mK readout hardware from magnetic fields / EMI
- Interface with detector modules, notably
  - Mechanical /thermal design
  - Bond pad pitch of readout -to-detector superconducting flex cable
- Design status: In progress

MUX & TES bias chips
High-density SC flexible cable
PCB for biases, row addressing
Si wiring chips

CMBS4 interface chip concept
SWH 12/8/20

Anderson, Derylo, Haller, Henderson, Hilton, Moncelsi, Schillaci, Sapozhnikov, ...
**100mK: Technical Design (2)**

**100mK TES Bias/interface/filter Chips**
- Shunt resistors to voltage-bias TESs
- Nyquist inductors to control TES bandwidth
- Simple fabrication and tuning of components
- Efficient warm screening for continuity, witness cold screening for component tuning
- *Design status:* Parameters need to be set, but a mature design exists for protos

**100mK Multiplexer Chips**
- First-stage SQUIDs to amplify TES currents
- Superconducting flux-activated switches to address rows
- *Design status:* Parameters need to be set, but a mature design exists for protos
- Challenges include throughput for production

*Photo: BICEP / H. Hui, L. Moncelsi, A. Schillaci*
4K: Technical Design

4K SQUID Array Amplifier
- Series array of SQUIDs that amplifies signal for transmission to warm electronics. **One per column**
- Requires magnetic shielding to suppress environmental fields and gradients at chip location
- **Design status:** Parameters need to be set, but a mature design exists for protos

4K SAA Board
- Each set of 8 SAAs (on simple carrier boards) packaged in a single compact shielded module.
- Each **4K board** contains 16 SAAs
- **Design status:** In progress

4K Mechanical Components
- Provides shielding, mechanical / thermal interfaces
- **Design status:** In progress

Open: **4K vs 1K. Some advantages to moving to 1K**
100mK & 4K Cables: Technical Design

100mK Mux-to-Detector Flex Cable
- **Superconducting** connection between detector wafer and Nyquist / Mux chips
- Dense **bond pad pitch** (interface to detector wafer). Currently set at 100um
- **Design status:** Not started
- **Challenges** include yield at desired signal trace pitch

100mK-4K Cable

4K-300K Cable
- Route signals from detector wafer to warm electronics
- Commercial **NbTi / Manganin** twisted-pair loom cabling with standard connectors *(Tekdata, other vendors)*
- Strong **interface** constraints: lengths from LAT/SAT design, impedance limits from readout performance
- **Design status:** Parameters need to be set, but a mature design exists for protos
**300K**: Technical Design

**Warm Readout Module Hardware & Firmware**
- Row boards provide row addressing signals
- Column boards provide all other signal generation (SQUID and TES biases), filtering, preamplification, conditioning, and digitization.
- Firmware provides PID SQUID controller, data transmission, and a control interface for the hardware.
- *Design status: Not started*

**Readout Software**
- Software provides low- and high-level user control over the hardware and firmware, interfaces with DAQ and Control
- *Design status: Not started*
**Optimization and system engineering** across DRM (also SAT, LATR) can help ensure noise, bandwidth, stability reqs met.

Readout noise equivalent power (NEP) set by:
- Detector resistance
- Mux chip SQUID design
- Aliasing, set by bandwidths below

**TES noise bandwidth** set by L/R time constant:
- Detector resistance
- Nyquist chip L, R
- Stray L, R from Detector, 100mK Readout, Module

**Readout bandwidth** set by impedances on two paths:

100mK SQUID - 4K SQUID
- Mux chip SQUID output impedance
- 4K SQUID amplifier input impedance
- Stray L, R from 100mK, 4K readout
- Cable lengths set by telescopes (LAT, SAT)

4K SQUID - Warm Electronics
- 4K SQUID amplifier output impedance
- Warm readout electronics
- Cable lengths set by telescopes (LAT, SAT)
Readout Deliverables Highlights

**Cryo 100mK electronics**
- 6.6 mm
- Si microfabrication, cryogenic testing
- MUX chips (~55,000)
- TES biasing chips (~55,000)
- RO units and Superconducting flex cables (~3000 each)
- **Custom fabrication, commercial procurement**

**Cold 1K/4K electronics**
- 5 mm
- 4K SQUID Array Amps (~8500)
- Shielded modules
- **Custom fabrication, cryogenic testing**

**Warm electronics**
- Custom fabrication, commercial procurement
- Row boards (~1000) Column boards (~1500)
- 100mK-to-4K cables, 4K-to-300K cables (~1500 each)
- **Custom fabrication, commercial procurement**
Workflow: Production/ Screening/ QA

Although this TDM design has vast heritage in deployed instrumentation, much large number of parts to be fabricated, especially superconducting circuits on silicon. Design/planning involves:

- **Modular component designs to enable high-throughput workflow of fabrication, QA and delivery**
- **Extensive in-process quality monitoring for microfab**
- **High-throughput screening of fabricated superconducting circuits at 4K in deployable packaging (100mK RO units, or 4K SAA modules)**
Summary/Conclusions

- CMB-S4 will implement DC voltage biasing and time-division multiplexed readout of its TES bolometers
- We have an implementation concept, some mature designs and preliminary parameters to use for prototyping based on Stage-2 and Stage-3 experience
- Engineering design for preliminary baseline has commenced where possible with limited resources, although mostly outstanding.
- Incorporating design features for ease of production, screening, QA
- DRM parameter optimization and system engineering can help avoid missed requirements. Ultimately, validation of design will come from testing the performance of prototypes.
Backup slides
**Amplify** TES signals
- 100mK SQUID
  - One per TES
- 4K Series SQUID Array
  - One per column

**Switch** among TESs
*Read rows one at a time*
- Josephson junction switches
  - One per TES

**Sample TES signals**
- Control readout system
  - ADCs, DACs
  - Real-time filtering
  - Interface to DAQ

**Supply stable voltage bias** to each TES
- Parallel shunt resistor
- Bandwidth-limiting inductor

More detail available in the CMB-S4 Readout Assessment materials and [backup](#).
CMB-S4: Time-division multiplexing

Interfaces to Detectors/Modules

- TES Detectors
- WBS 1.03
- Cryo 100 mK Electronics
- WBS 1.04.03
- Mux to Detector
- Flex Cables
- Nyquist Chips
- Mux Chips
- Nyquist Boards
- Mux Boards
- 100 mK Assembly, Test, Shipping

Interfaces to SAT, LAT

- WBS 1.04.04
- Cold 4K Electronics
- 1.04.04.01
- SQUID Amplifier
- 1.04.04.02
- SQUID Board
- 1.04.04.03
- Mechanical Components
- 1.04.04.04
- 4K Assembly, Test, Shipping

Interfaces to SAT, LAT, DAQ

- WBS 1.04.05
- Warm Electronics
- 1.04.05.05
- 4K - 300K cables
- 1.04.05.02
- Readout Module
- 1.04.05.03
- Readout Module Firmware
- 1.04.05.04
- Readout Module Software
- 1.04.05.06
- Readout Crate
- 1.04.05.07
- Warm Assembly, Test, Shipping
- Cold & Cryogenic Component Operation
- TES Bias
- TES Signal Readout
- FPGA
- DAC
- ADC

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### Driving Interface Highlights

- **Detectors:**
  - Electrical connection via wire-bonds
- **Modules**
  - Mechanical/shielding packaging of 100 mK Cryo into detector module
  - Thermal power dissipation
- **LAT/SAT**
  - Mechanical volumes for 4K Cold inside cryostats & 300K Warm outside
  - Electrical effects of cable run lengths
  - Thermal interfaces with cryogenic system
- **DAQ**
  - Electrical connections to DAQ data ethernet
  - Software/control/telemetry connection to observatory control system in DAQ

Numbers in table above are **DocDB ids.**

Ongoing refinement of associated specifications/levels before CD1.
DRM parameter optimization example

Stable, overdamped TES operation

Osherson, Filippini

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