Readout System Design Status

Gunther Haller (L2 CAM) for WBS 1.04

Parallel Session, Tuesday, March 9, 2021

MCE Electronics (obsolete)

A fully-kitted subrack contains:

- 1 clock card
- 2 (48-HP subrack, 3 MDM connectors) or 4 (72-HP subrack, 5 MDM connectors) readout card signals
- 3 bias cards (in some situations one might be removed)
- 1 address card

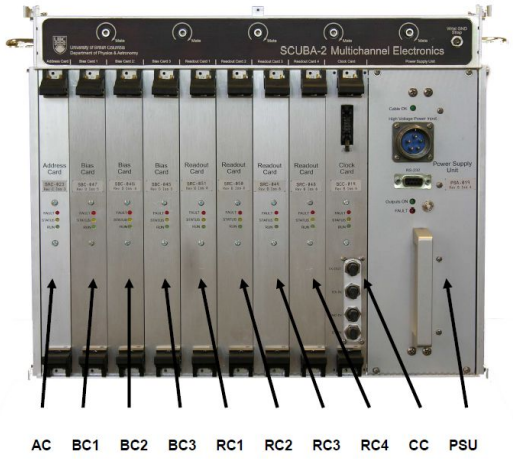


Figure 2.1 MCE subrack with switching power supply card.

What we have in MCEs for S4 test setups*:

- SLAC: 3 MDM with one 41-row and two column cards
- UCIC: 3 MDM with one 41-row and two column cards
- (ANL->FNAL): 5 MDM with one 41-row and one column card

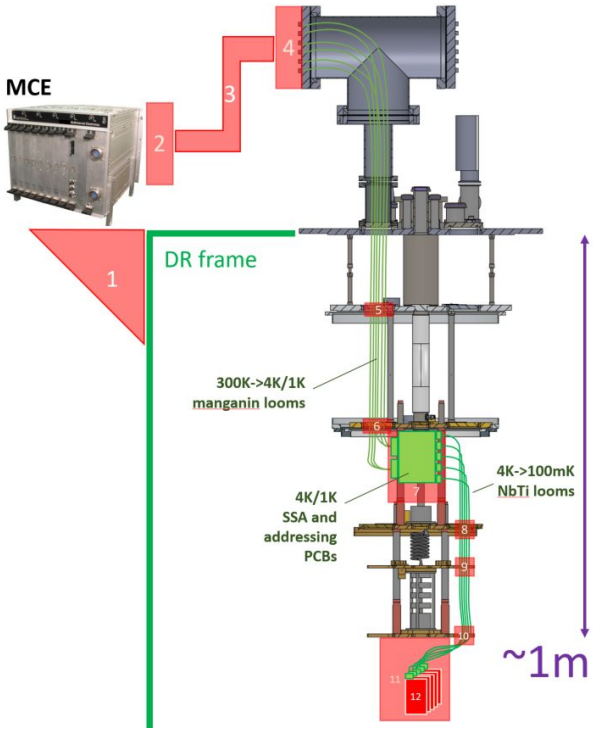
What we can read out without making modifications to setups which is not recommended for develop cold harnesses and software to use spare DACs on column cards for extra rows)

- **<u>41 of the 64 rows of TES columns</u>**
  - => switch cables between flange connectors to read out row 1-41 versus 42-64
- **<u>Two 100mK modules each reading out one of six wafer sides</u>**
  - => switch cables between flange connectors to read out other wafer sides

MCE support needed tbd

Ok for initial testing, but limits what can be tested, requires multiple test cycles

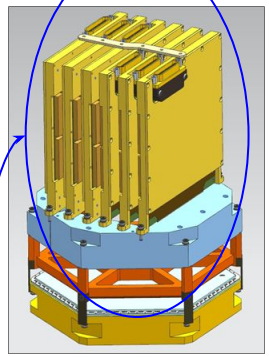
- **Goal to replace MCE electronics with new electronics as soon as feasible**
- **Goal to build the test-ups so only 100mK modules need to be replaced to result**



*Not clear if there are spare column cards available from other experiments to augment

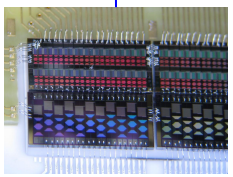
CMB-S4 implementation

Anderson, Benson, Derylo



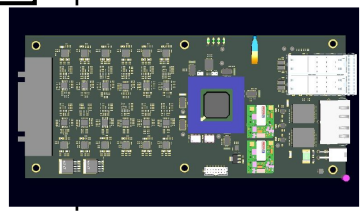
100mK Readout units on Detector module

For first version test-stand, Readout modules are on same level as wafers as opposed to on top

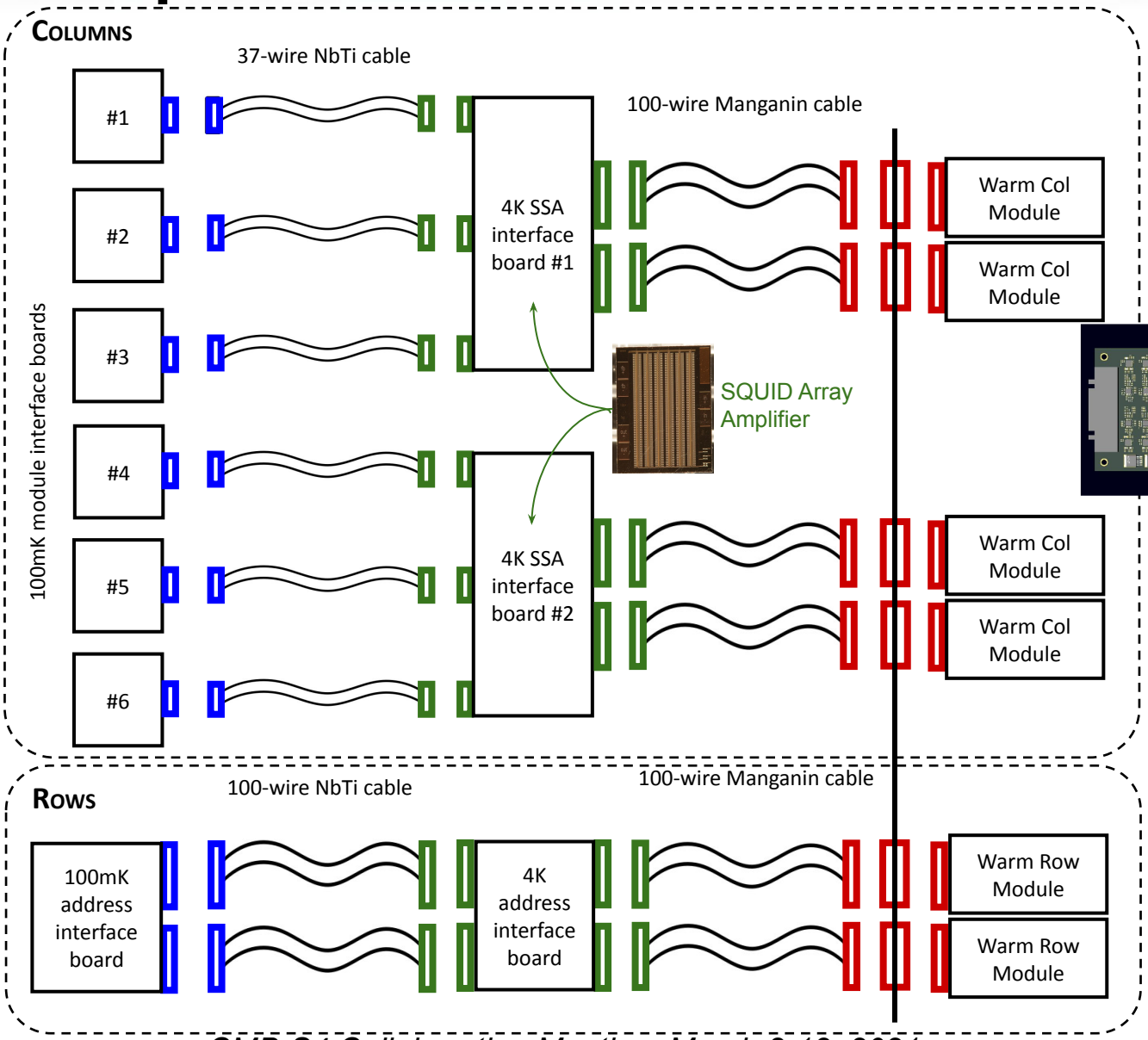


SQUID multiplexer and TES bias chips

Cryogenic cabling

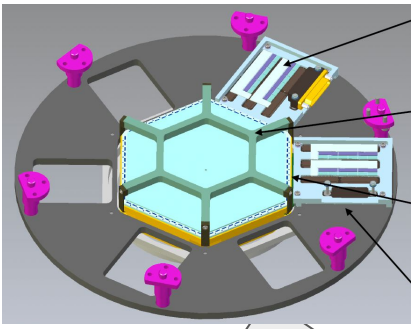


Warm electronics modules



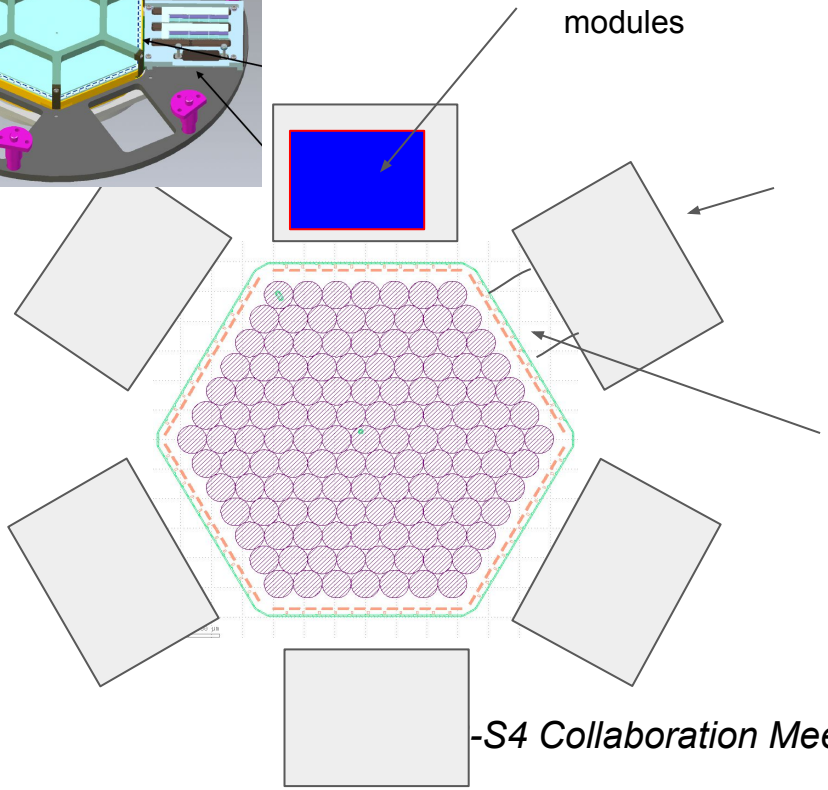
CMB-S4 Test-Stand: Bluefors dilution fridge instrumentation cartoon

- Room temperature parts: (1-4)
- Heat sinks for manganin looms: (5-6)
- 4 Kelvin SSA PCB prototype and addressing PCB bracket(s) (7)
- Heat sinks for NbTi looms: (8-10)
- 100 mK modules PCB prototypes and addressing module brackets (11-12)



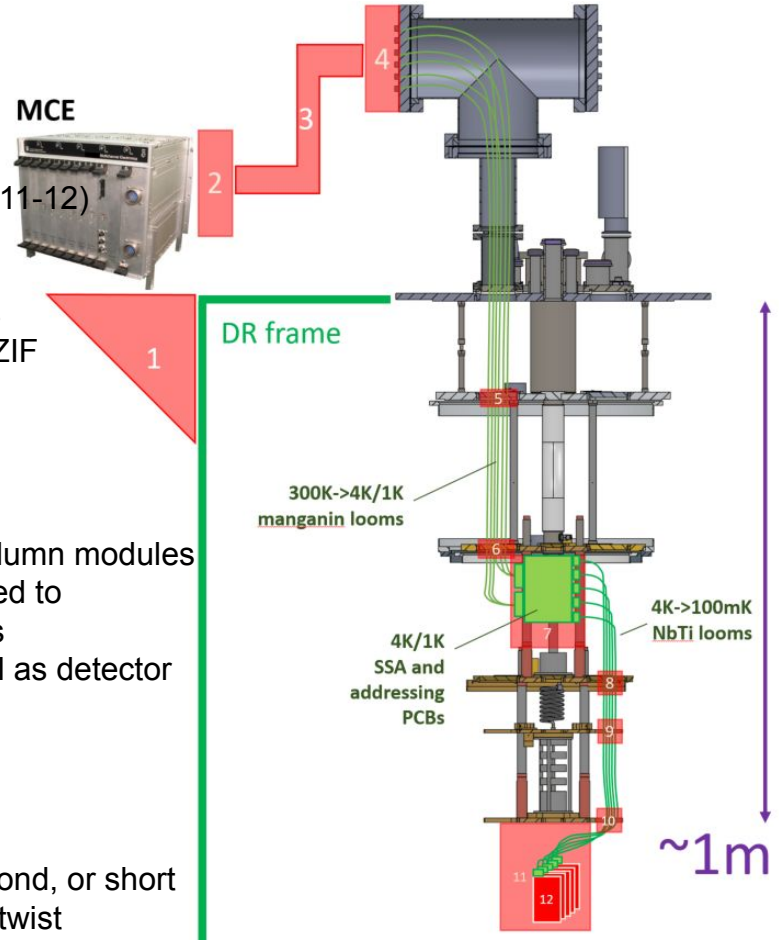
A. Anderson, B. Benson, G. Derylo,

100mK row address modules mounted to column module. ZIF cables to chain all column modules



100mK column modules wire bonded to flex/wafers
same level as detector wafers

Direct bond, or short flex, no twist

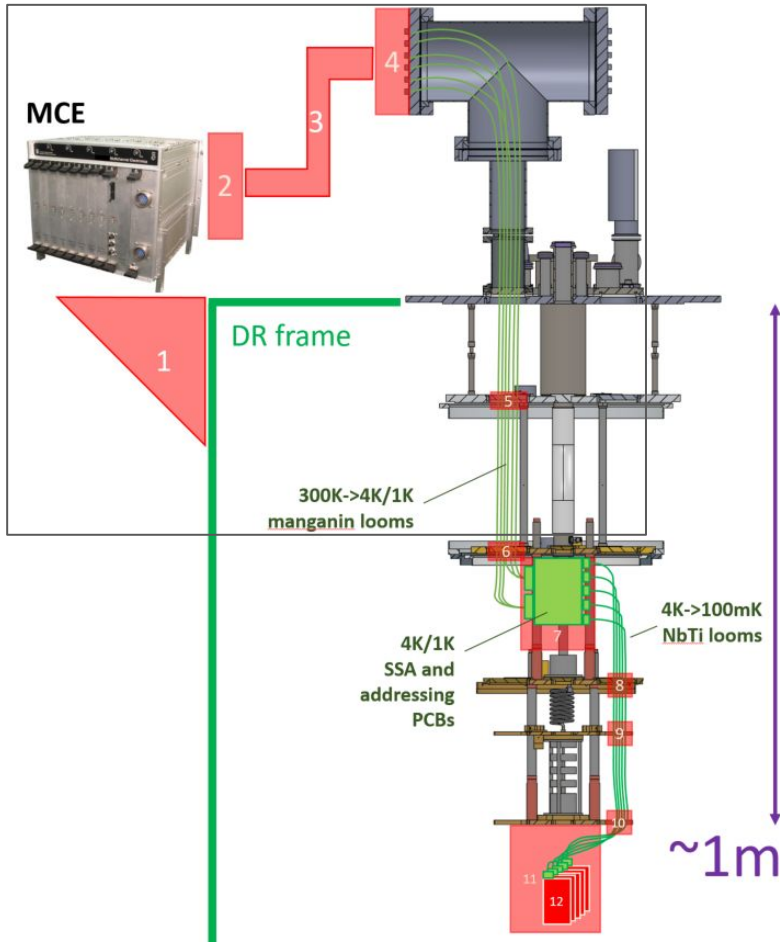


Readout supplies modules to “Module Assembly” L2 with short cables already bonded (unless direct bond)

Warm Components Status

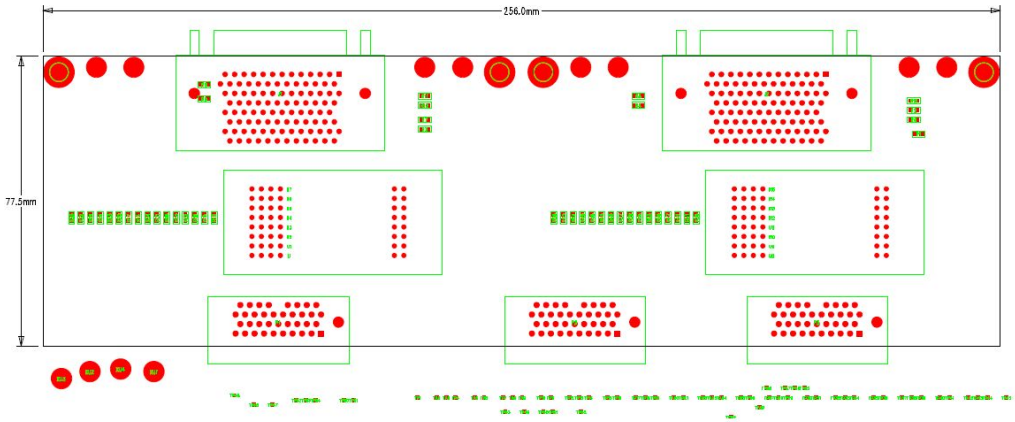
Warm Electronics

- MCE: at SLAC, UIUC, FNAL
  - 41 row out of 64 row readout
  - One or two wafer side readout (unless more column modules can be found)
- Or new row and column electronics modules (upgrade), see separate presentation at this meeting
- 300K RF-shield/connection from vacuum feed-thrus to MCE (started design)
- Vacuum flange with connectors (ordered, but 100 days delivery, trying to expedite)
- Connectors and cables
  - Glenair 300K cables (only needed for MCE): Cable designed, quote received, about to order
  - Glenair connectors ordered for cold cables (end of March delivery)
  - Tekdata superconducting cables: Got quotes, but expensive
    - Needs to be placed by the time Glenair connectors arrive

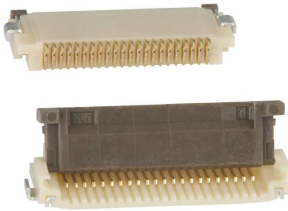


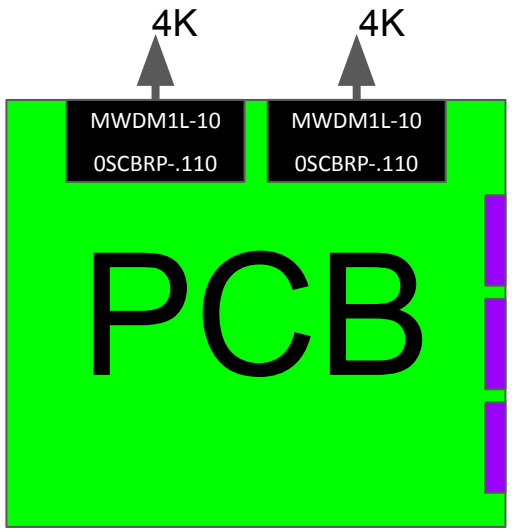
4K SSA module and 100mK Row select module

- Schematic complete and reviewed
- Layout started
- Will use bare board on support bracket in chamber
- Mechanical enclosure design when FY21 funds arrive
- SSA chips to be supplied by ANL to NIST for SSA module assembly, chips being screened at ANL.



4K SSA board





ZIF ribbon cable connectors .

100mK row Address board

- 100mK row address board/module (elex/mechanical)
- Schematic complete

100mK column readout module

Several options on how to construct the 100mK Readout module

For superconducting signal connections

- Alumina board with Al traces
- Si wiring chip with Al or Nb traces
  - Nyquist and Mux chips mounted on Si wiring board
  - Nyquist and Mux chips mounted on ceramic carrier
  - Si wiring board for several columns or just one

Engineering trade study will include

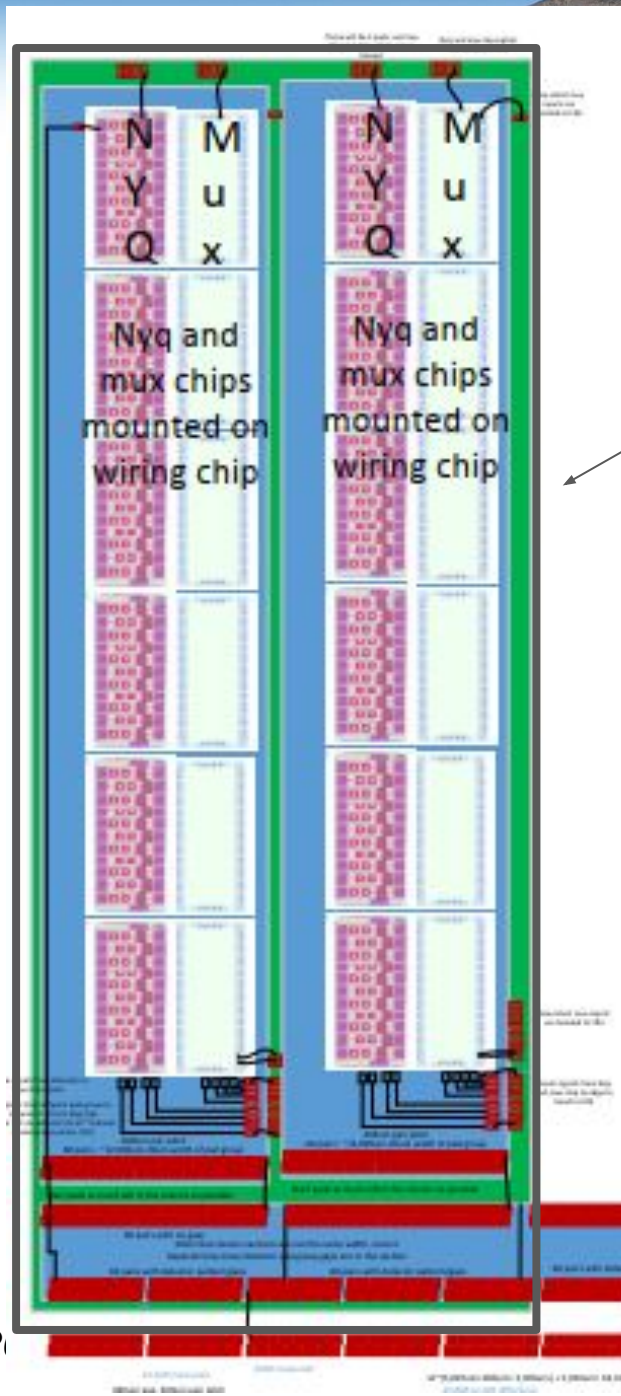
- NRE and production cost, manufacturability, complexity, risks, mechanics, space, thermal, performance, yield, reliability to decide on the best overall solution, needs some more time.
- Meanwhile Readout is designing one of the options in order to provide a solution to read out the CDFG wafers with the time and budget constraints while still being on the path for a production module.

2 column prototype for CDFG wafer

Design/fabricate two Si wiring chips (single layer, superconducting)

- Bonding pad pattern adapter chip: Small chip at bottom spanning two columns
  - Adapts wafer pad pattern to pattern required by a column
  - Wafer has 12 groups of pads with 11 gaps
  - Column board has 5 groups
- Column wiring chip: Connects detector TES signals to Nyquist filter chips. One Si wiring chip per column
- Nyquist and Mux chips are mounted on top of the Si column wiring chip

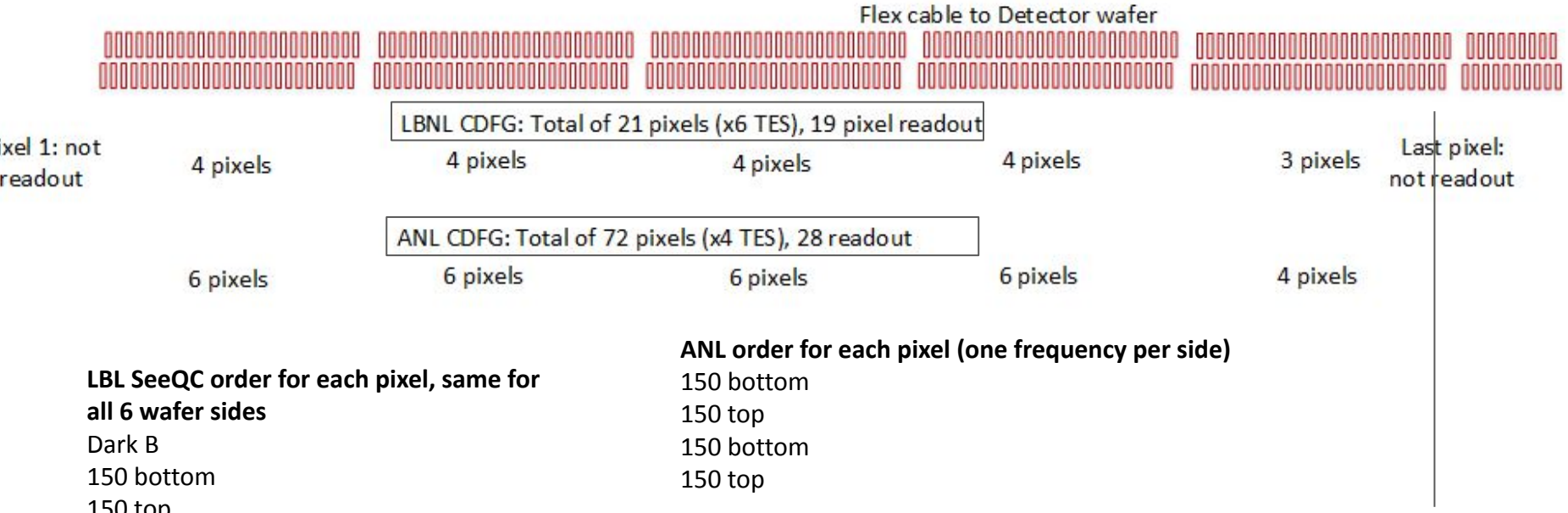
CTE mismatch is being addressed, there are several options



Pixel readout for CDFG wafer

With this 2 column module the following number of pixels can be read out on each detector wafer side:

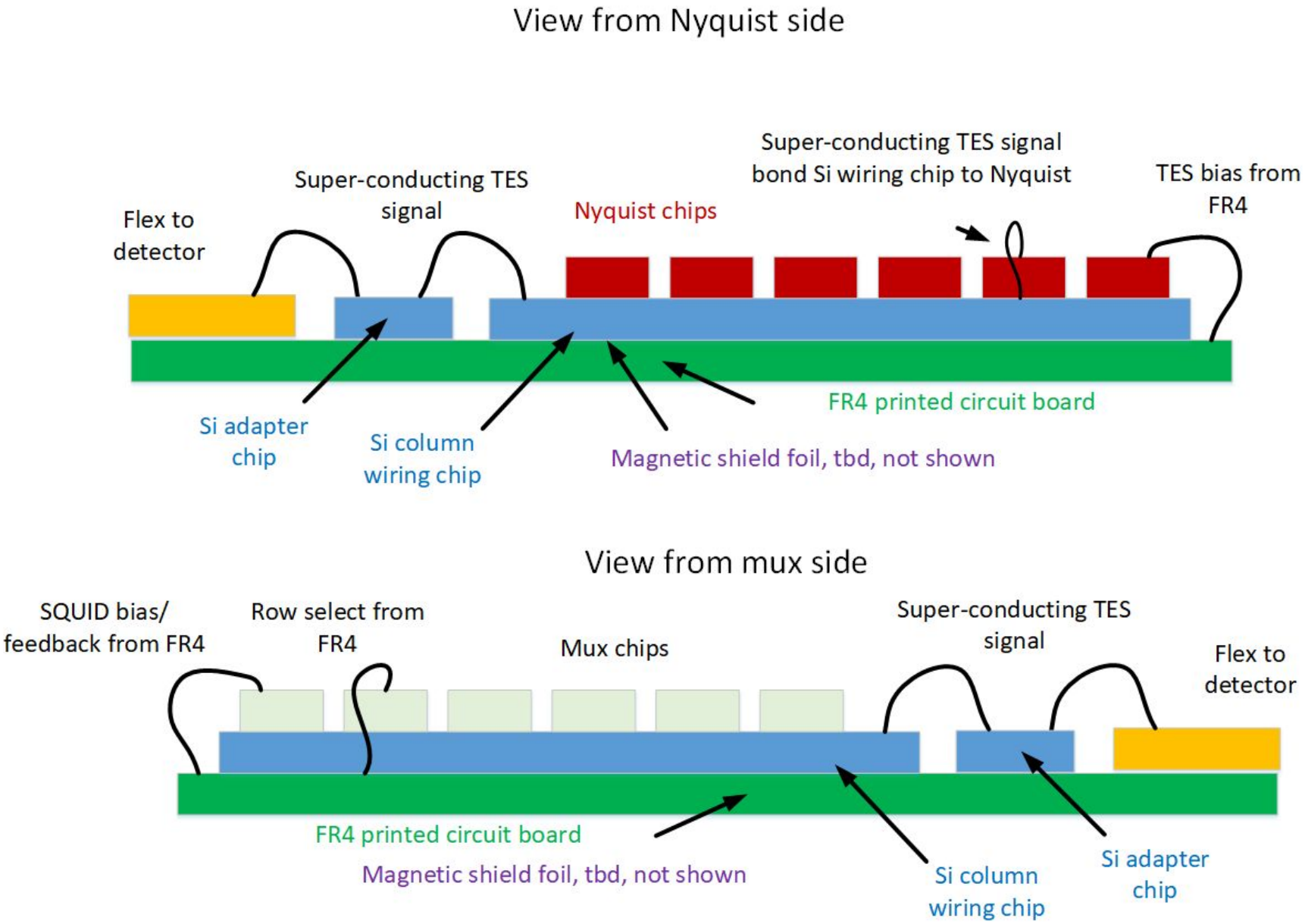
- Note that LBNL wafer has 2 darks per pixel which are on pads usually used for optical TESes. Pixel TES colors will not be on same bias but that does not matter for CDFG wafers.



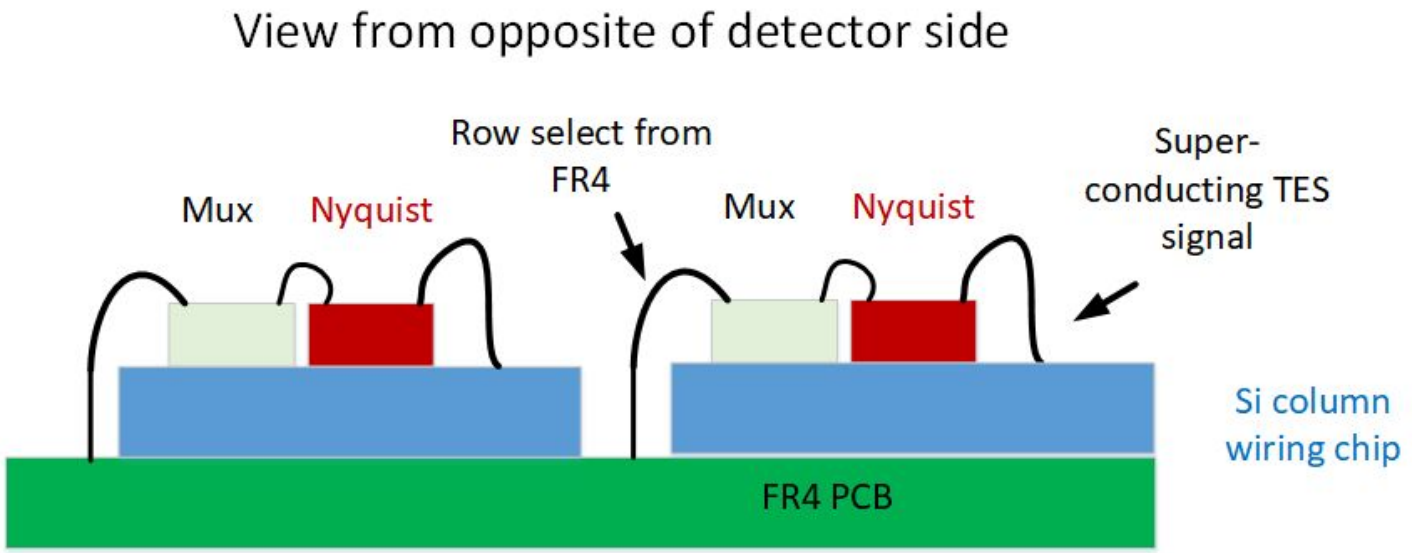
LBL SeeQC order for each pixel, same for all 6 wafer sides
Dark B
150 bottom
150 top
Dark A
90 bottom
90 top

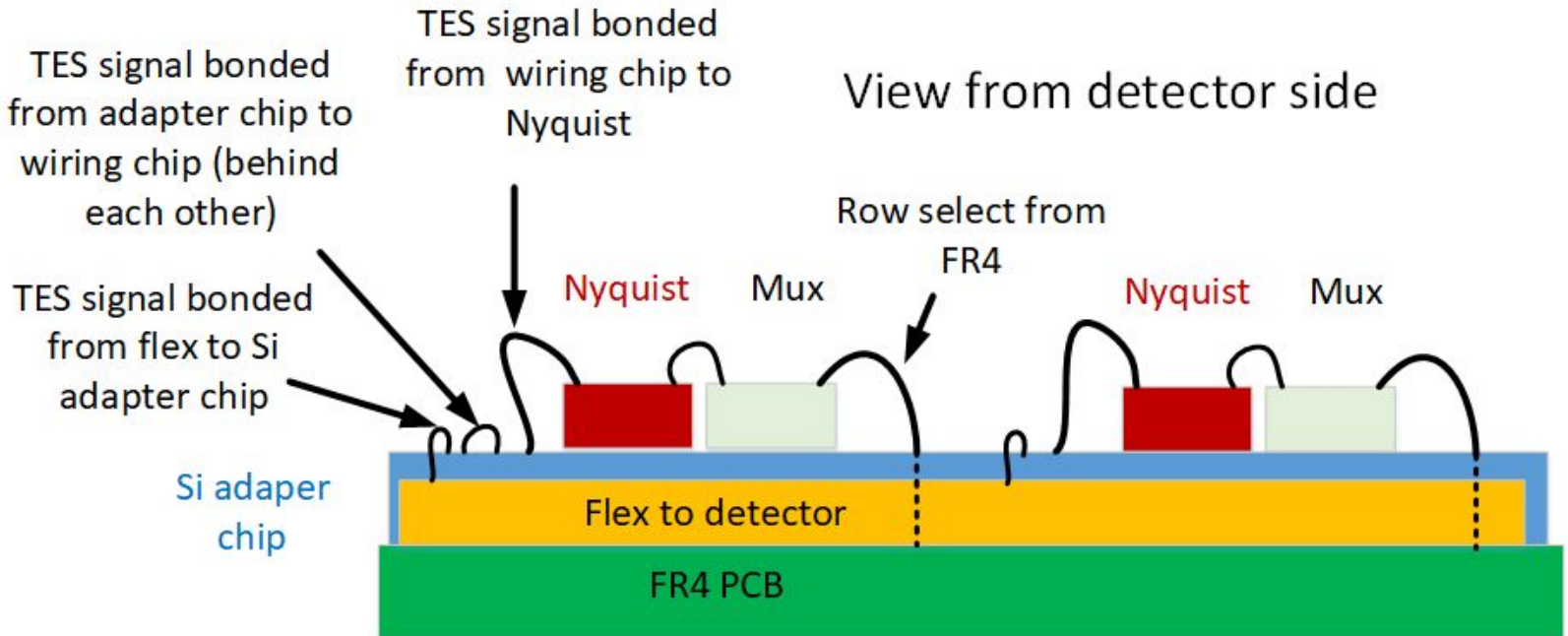
ANL order for each pixel (one frequency per side)
150 bottom
150 top
150 bottom
150 top
…
or
90 bottom
90 top
…
with Dark as the first pair of the 25-pair group

View from Nyquist and Mux side (just for reference)



View from detector and opposite detector sides (just for reference)





Nyquist-Filter Chips (NIST)

In order to accomodate alternating frequencies at detector wafer pad interface:

- 11-channel Nyquist chip with two TES biases IO's
  Alternating TES'es inputs get alternating TES bias

Example for Detector wafer pad order (6 pixels/group)

- Dark, 90B, 90A, 150B, 150A, 90B, 90A, 150B, 150A, 90B, 90A, 150B, 150A, 90B, 90A, 150B, 150A, 90B, 90A, 150B, 150A, 90B, 90A, 150B, 150A; Dark, 90B, 90A...

- Nyquist chip channel order would then be (Red and Blue: Biases)
  - XXYYXXYYXXD YYXXYYXXYYD XXYYXXYYXXD etc

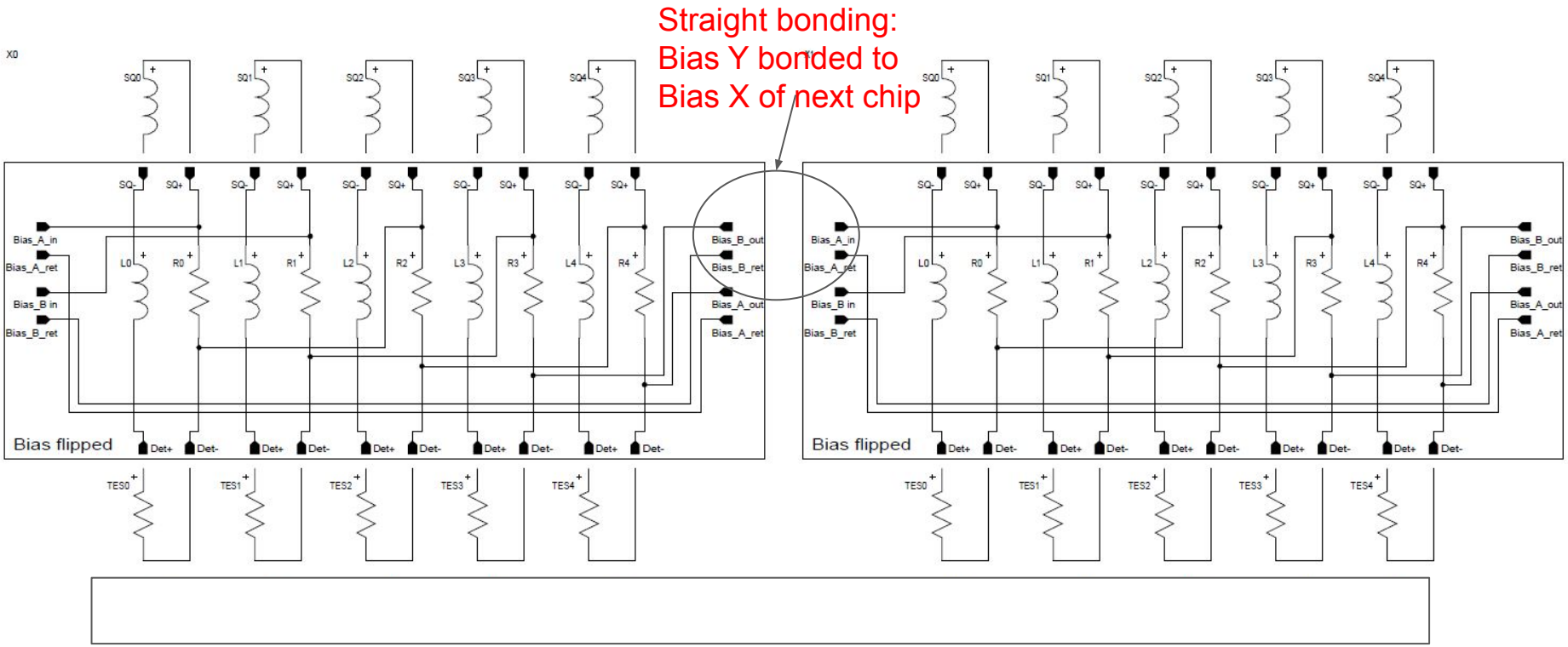
If detector wafer has only one frequency per detector wafer side:

- Program (software) the two Digital-to-Analog Converters in warm electronics to the same bias.

Nyquist Chip for S4 prototyping

Interleaved bias version, flipped bias leads
Keep 11 channels (below just shows 5). 11th would be used for Dark SQUIDS or Dark TESes (“D”)
First chip has color X as the first TES channel, second chip has then the first TES channel color Y. 3 chips in series would be:

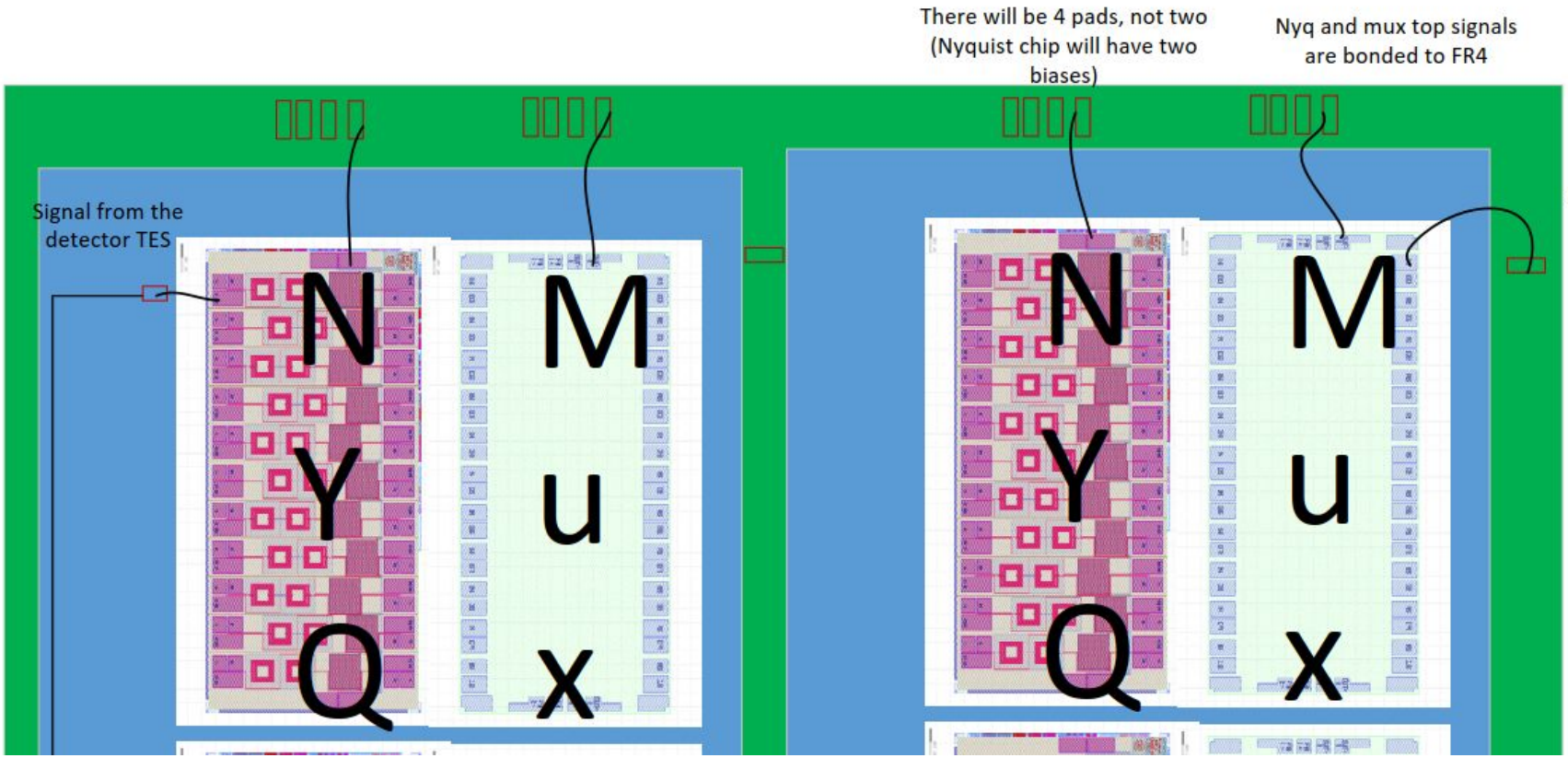
- XXYYXXYYXXD YYXXYYXXYYD XXYYXXYYXXD ..



Backup

Top part

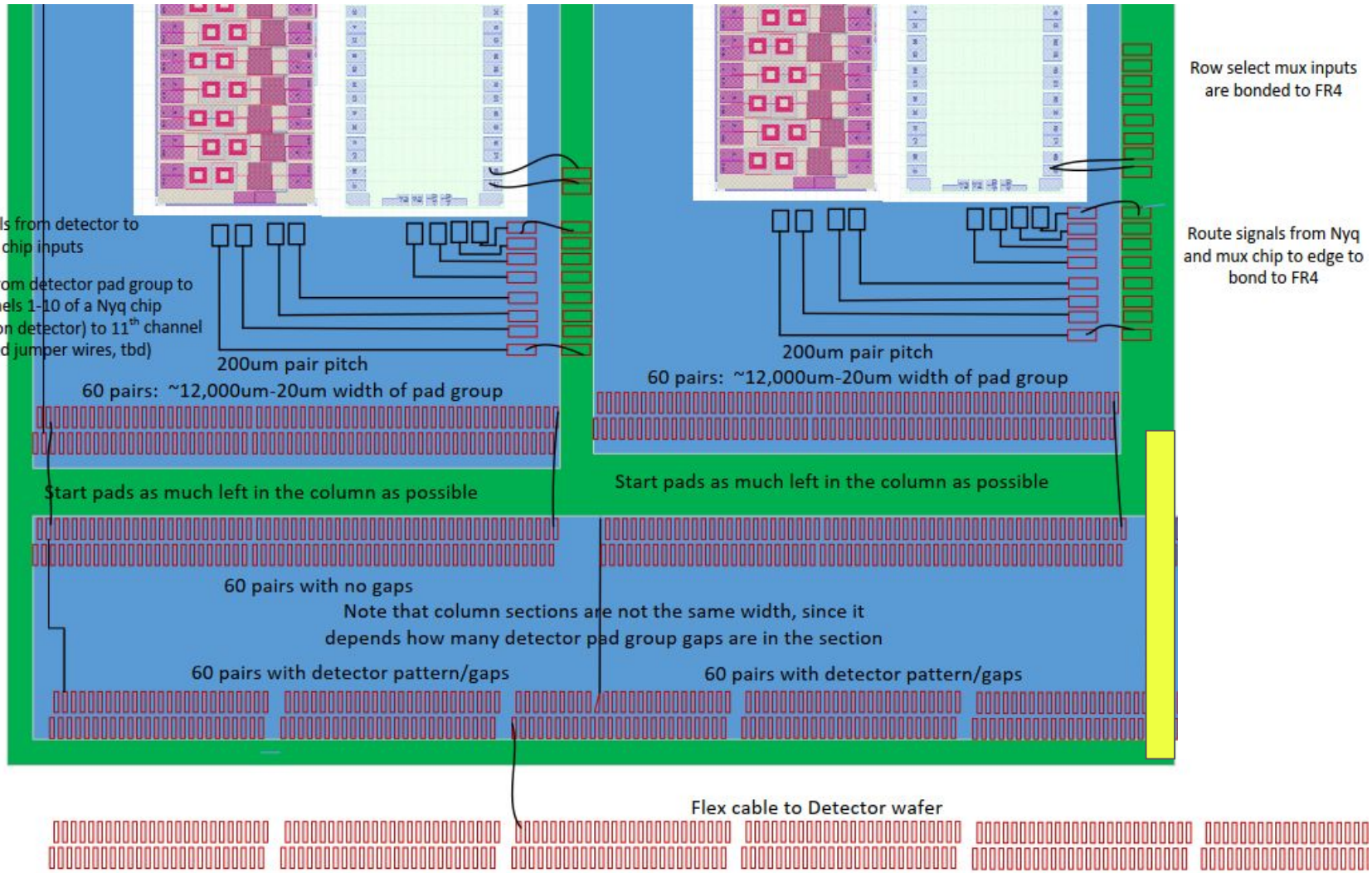
Green is FR4 PCB



Bottom part, 2-column version

Si column wiring chip

Si adapter chip



100mK readout Module with b: T-shaped Si wiring chips, shown (or a: rectangular)

Two options:

b: Marcor ceramic carriers mounted onto FR4 and Nyq and Mux chips mounted onto ceramic carrier Si chips mounted onto FR4.

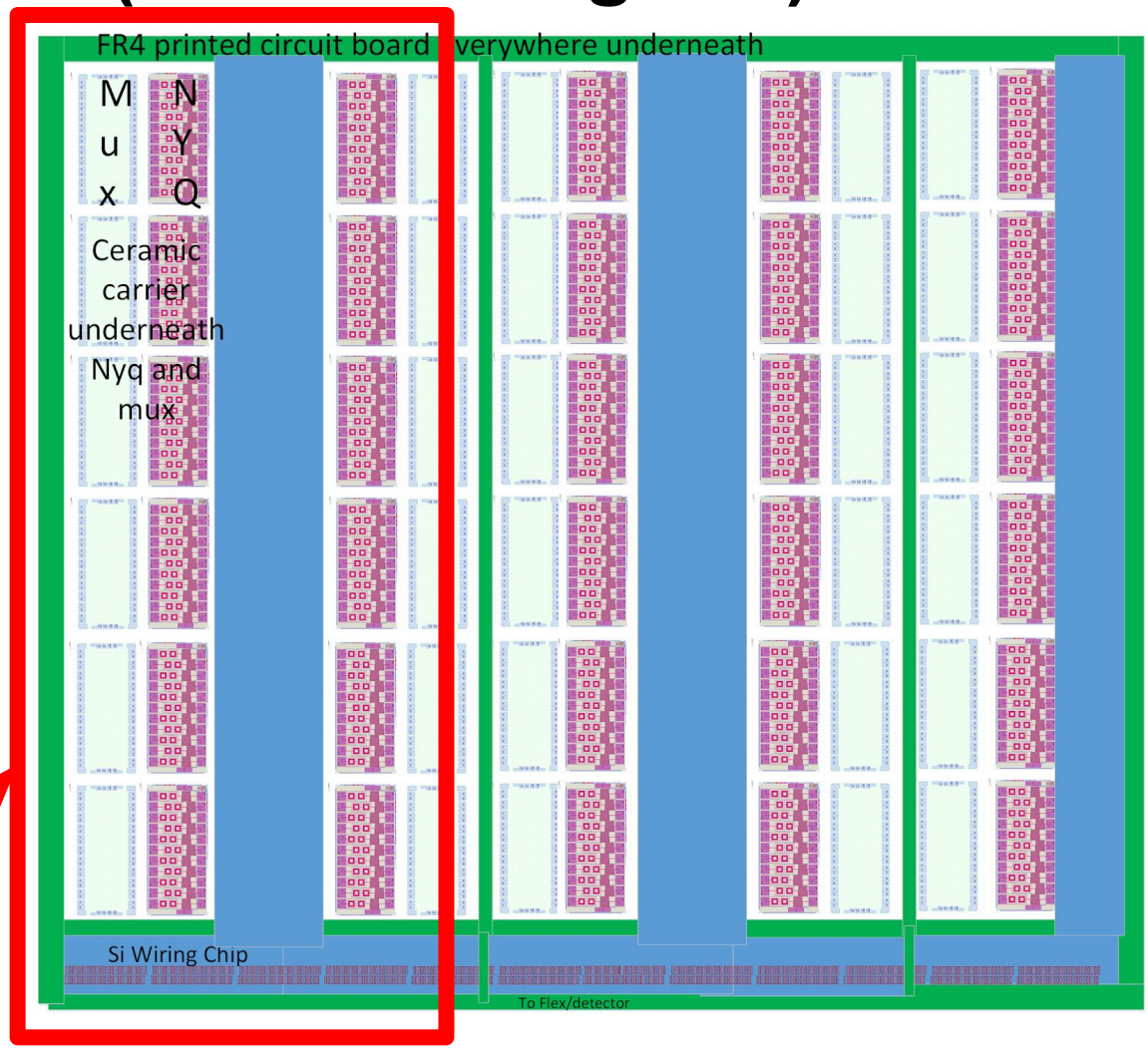
a: Si wiring board mounted onto FR4. Nyq and Mux chips mounted directly on the Si wiring chip.

Both match bonding pad pattern on CDFG wafer. For prototype just a, b is just laser-cut version of a

Wiring chip and FR4 board in schematic design

Two-column Readout board for prototyping and CDFG wafer readout (see next slides)

Magnetic shielding not shown

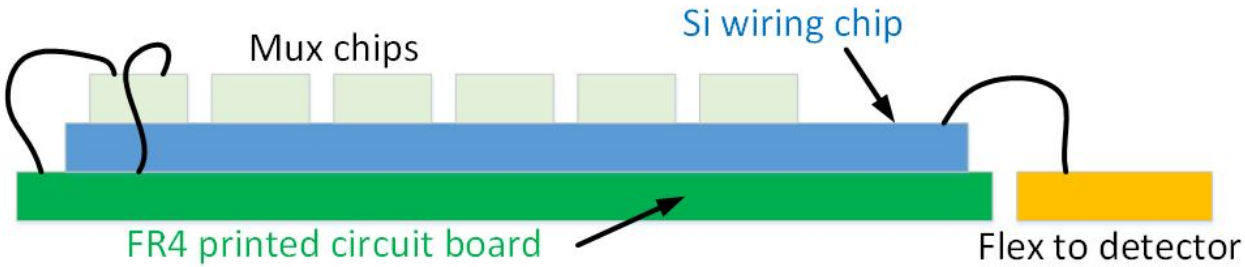


To Detector wafer

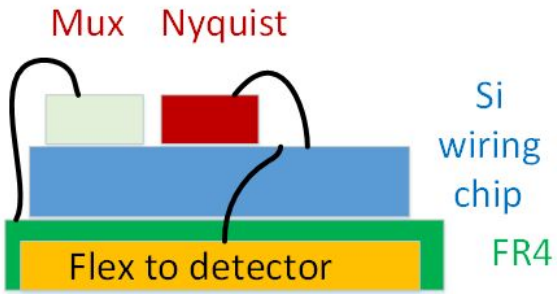
a: Nyquist and Mux chips mou
wiring chip

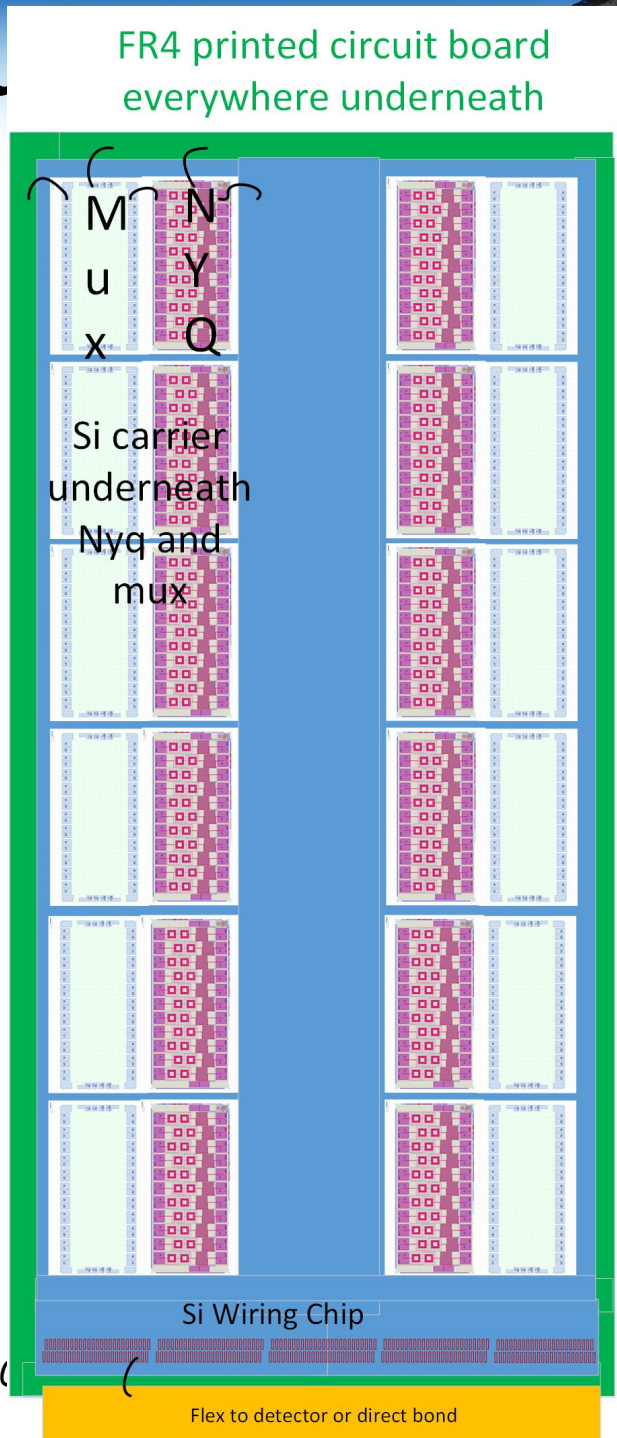
Si wiring chip a rectangle (can be saw cut on wafer)
Nyquist and Mux chips on Si carrier
All of it on FR4 PCB

Cross-section looking into left side of assembly (not to scale)



Cross-section looking from the detector into assembly



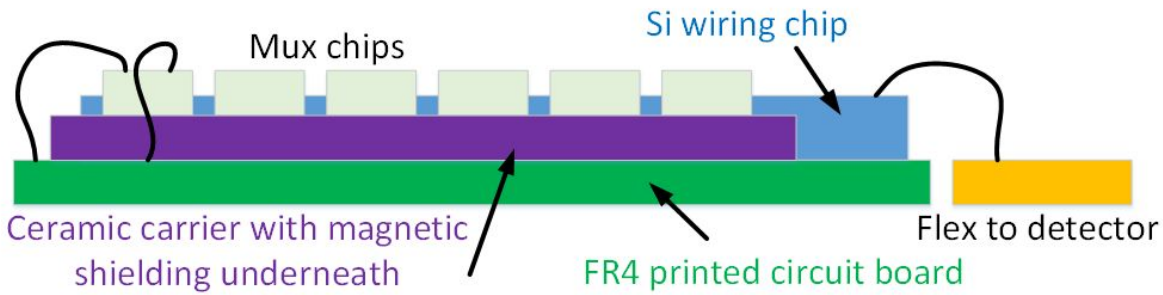


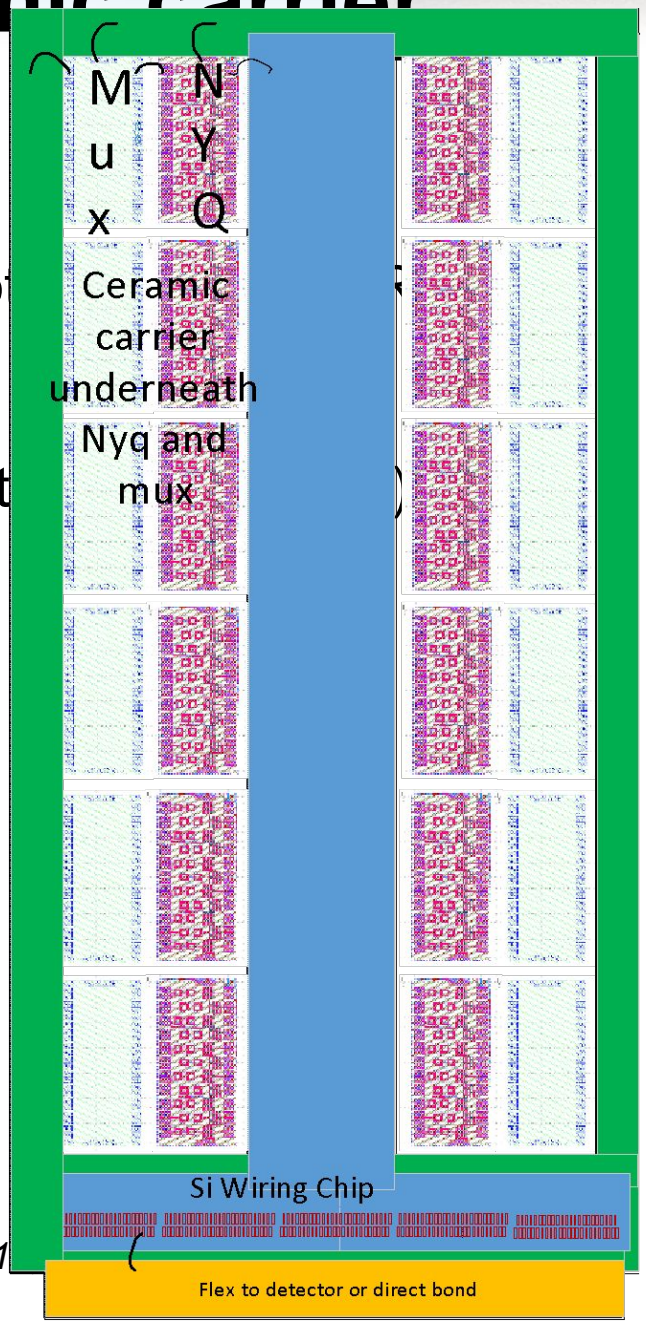
b: Si Wiring Chip and ceramic carrier

Si wiring chip an upside “T”
Nyquist and Mux chips on ceramic carrier
Si wiring chip and carrier next to each other, bo
All of it on FR4 PCB

(This is the same wiring chip as in option a, just

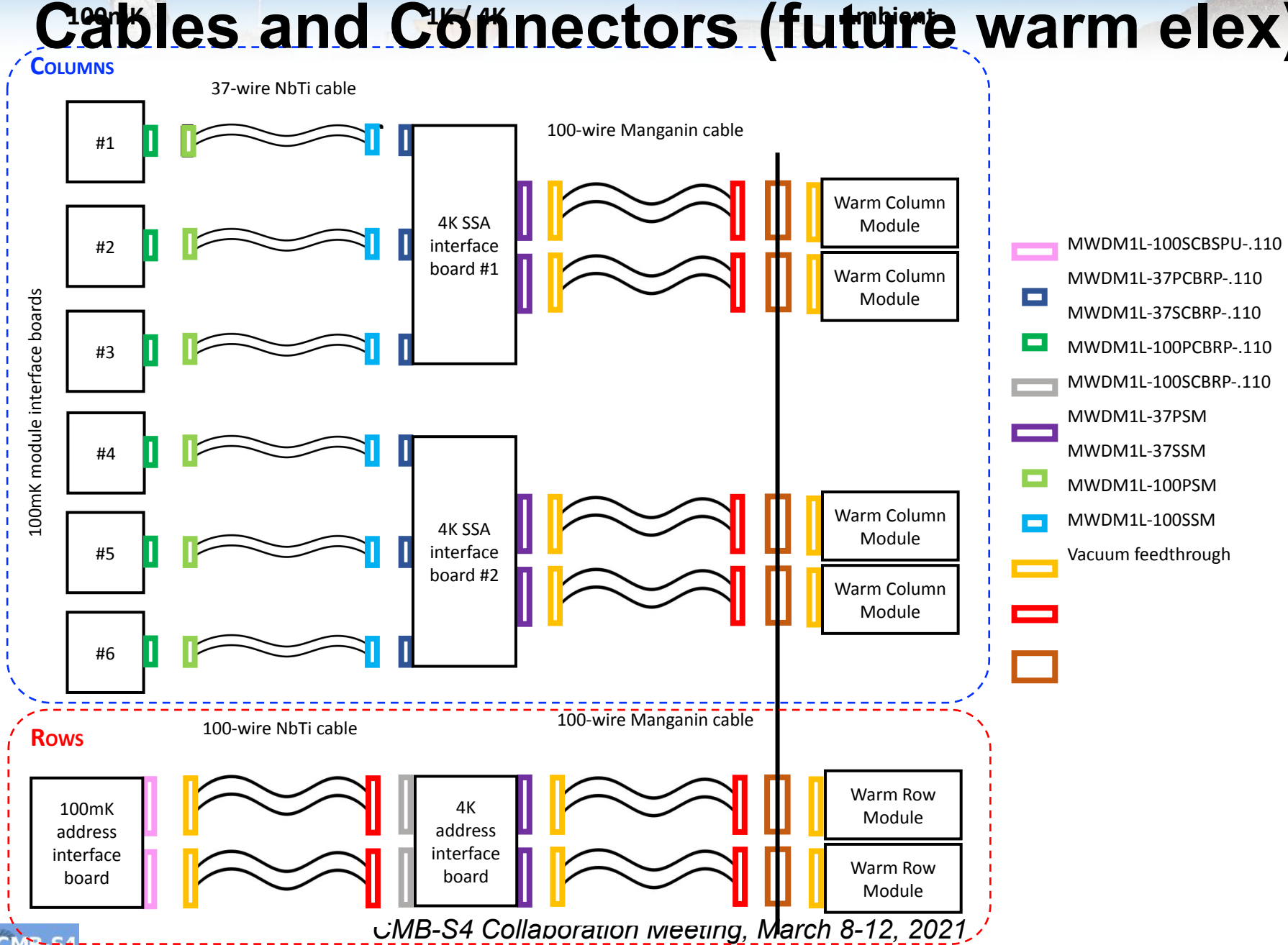
Cross-section looking into left side of assembly
(heights not to scale, just for illustration)



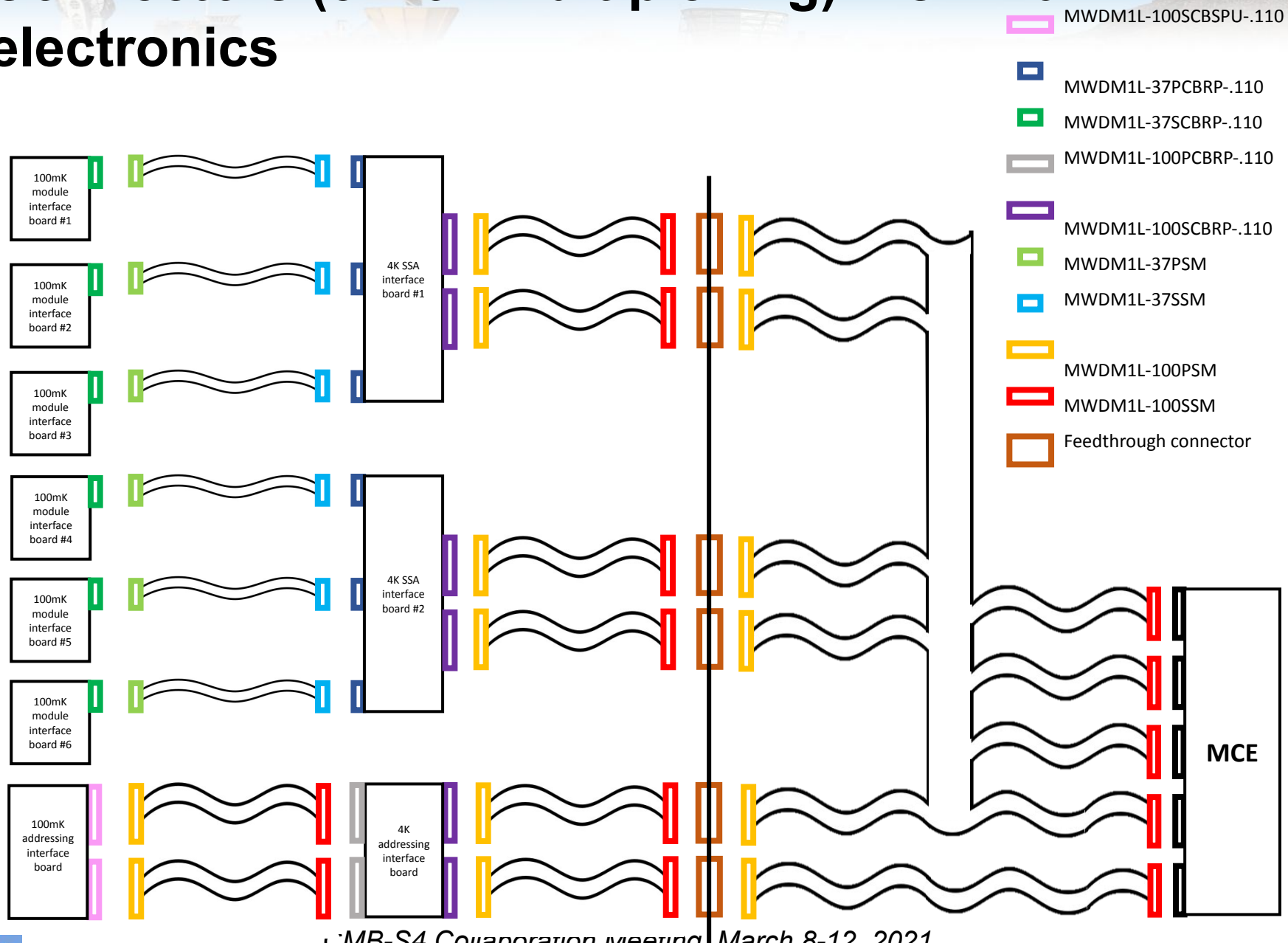


The nyquist/mux chips from 3" wafer fab are 380 um thick. The ones from 6" wafers will be 500 um thick

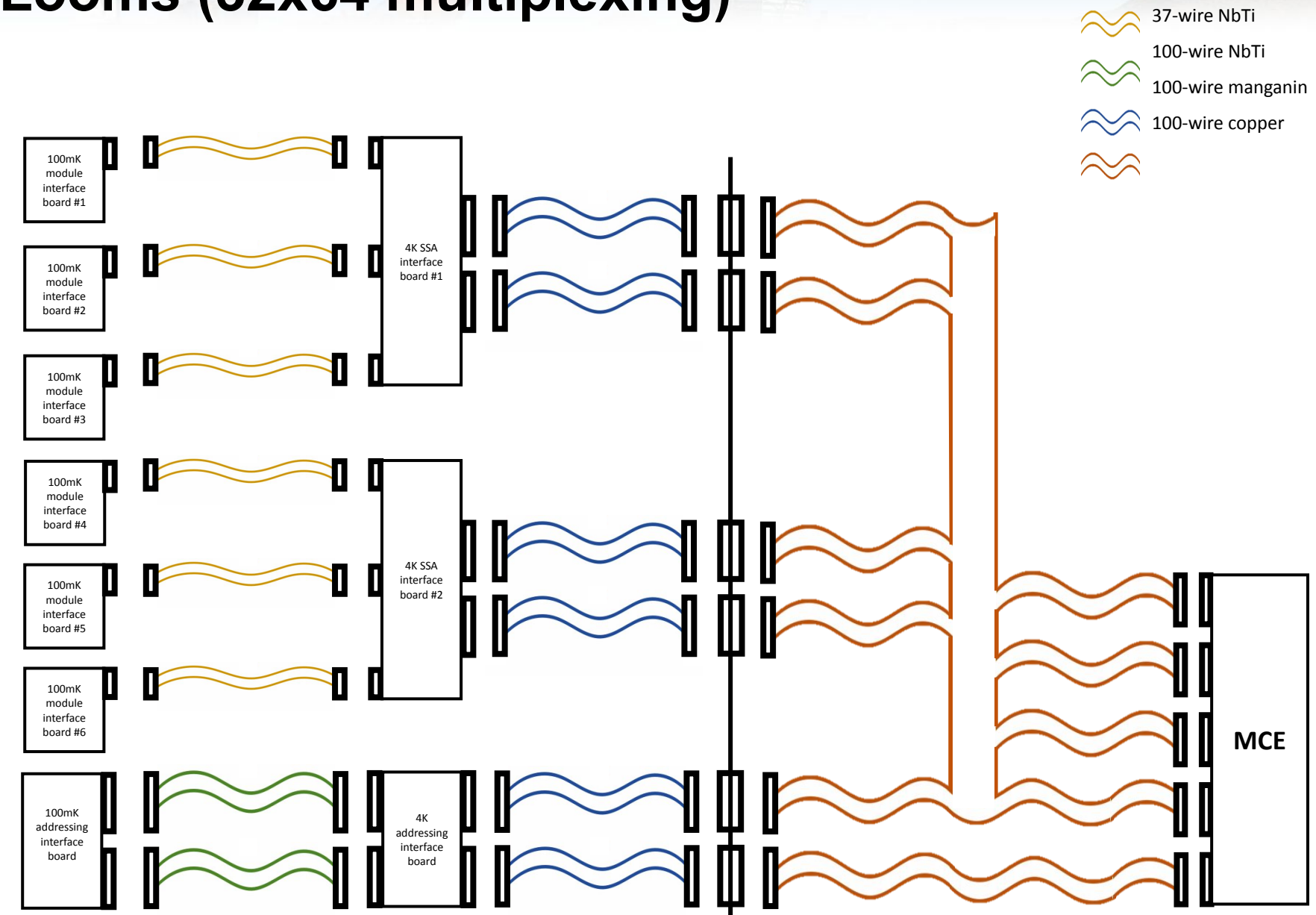
Cables and Connectors (future warm elex)



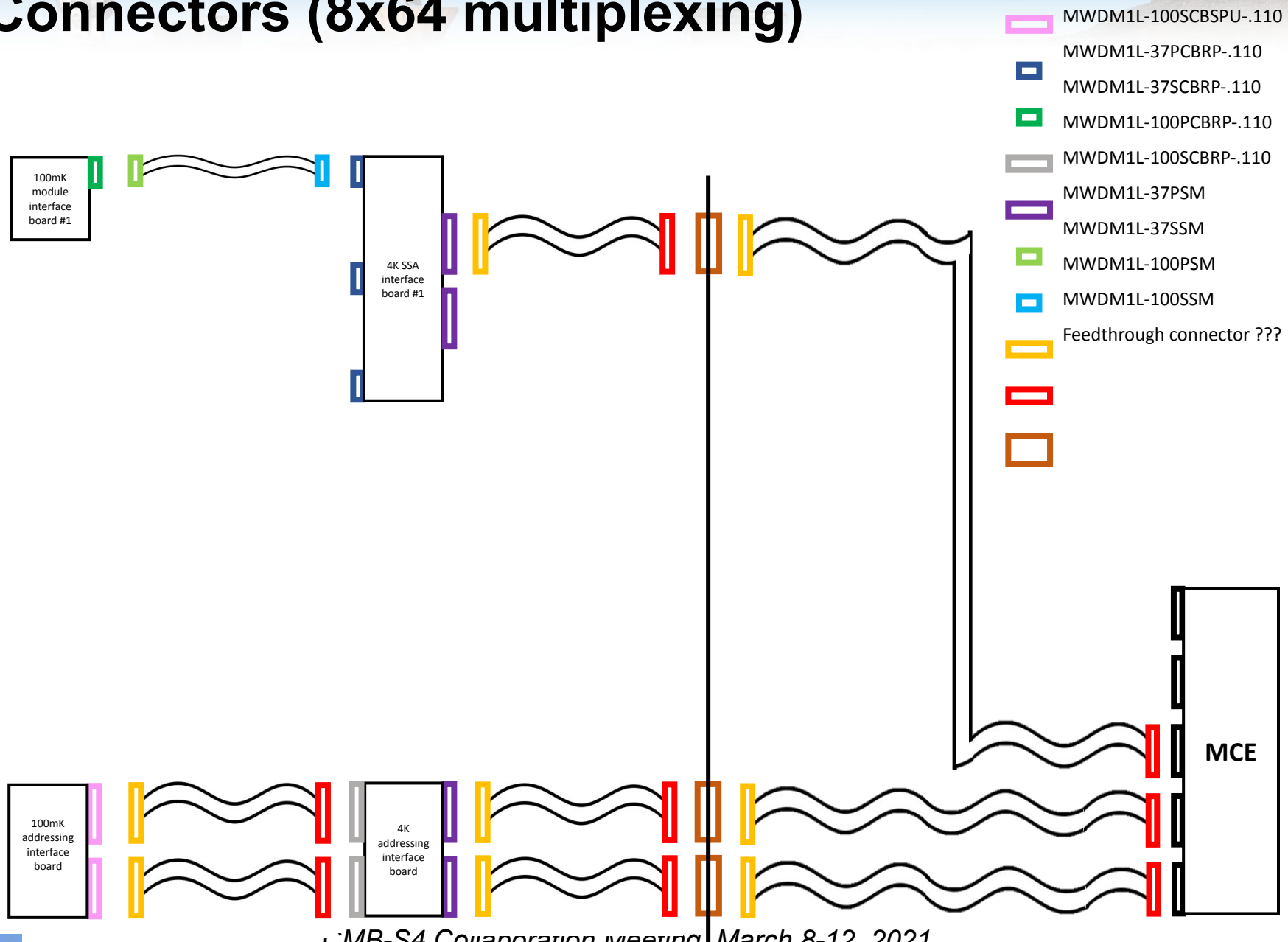
Connectors (32x64 multiplexing) MCE warm electronics



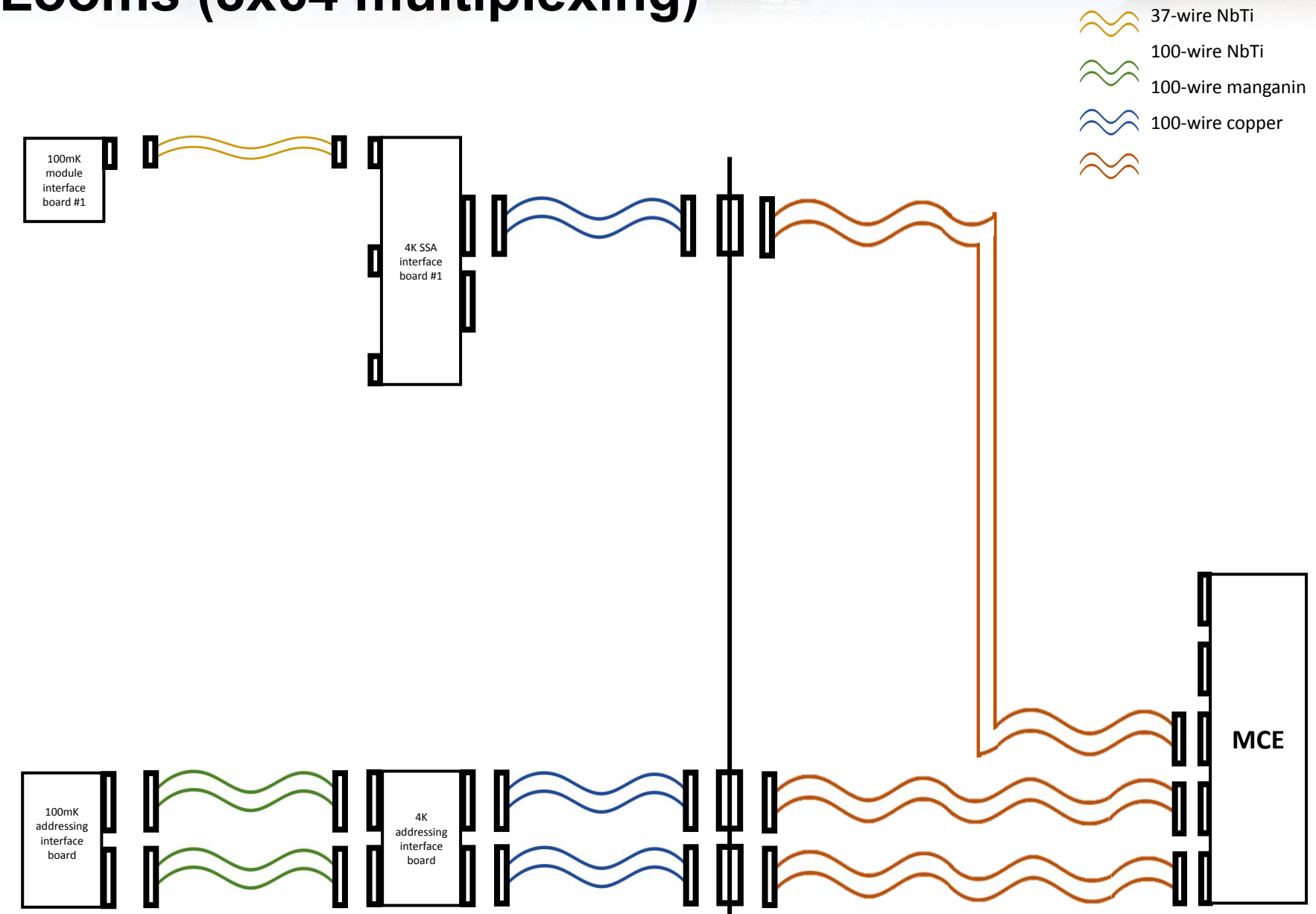
Looms (32x64 multiplexing)



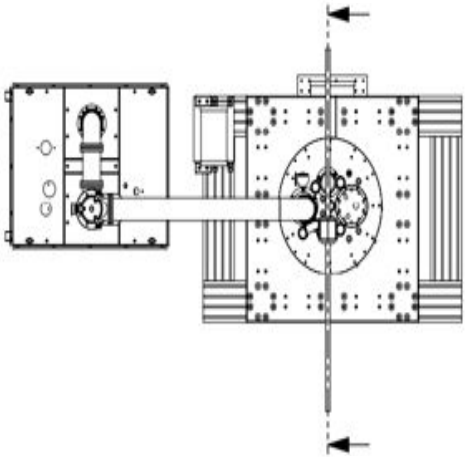
Connectors (8x64 multiplexing)



Looms (8x64 multiplexing)



Looms in a Bluefors LD400 (Shawn)



For comparison:
AdvACT test dewers had 6.9m roundtrip wiring between MCE and 4K SSAs. Here specifying 4m roundtrip if using MCE + 300K copper cables, 2.5m if using SLAC boards and no 300K copper cables.

750 mm
300K
Copper looms

Toki+Ed's 2x6
MDM100 f/t

~ MCE
(not to
scale)

~ MCE
(not to
scale)

I was imagining we'd be mounting up to 2x MCEs in these two positions when spec'ing out 300K copper loom lengths

Search documents and file names for text

1250 mm
300K->4K/1K
Manganin looms

900 mm
4K/1K->100mK
NbTi looms

FYI : This model is the SLAC DR which has longer tails than the standard LD400.

300K 100-way copper cables

Have not explicitly asked if we can supply connectors for them to make the assemblies with, if that's a consideration.

Manufacturer : Glenair

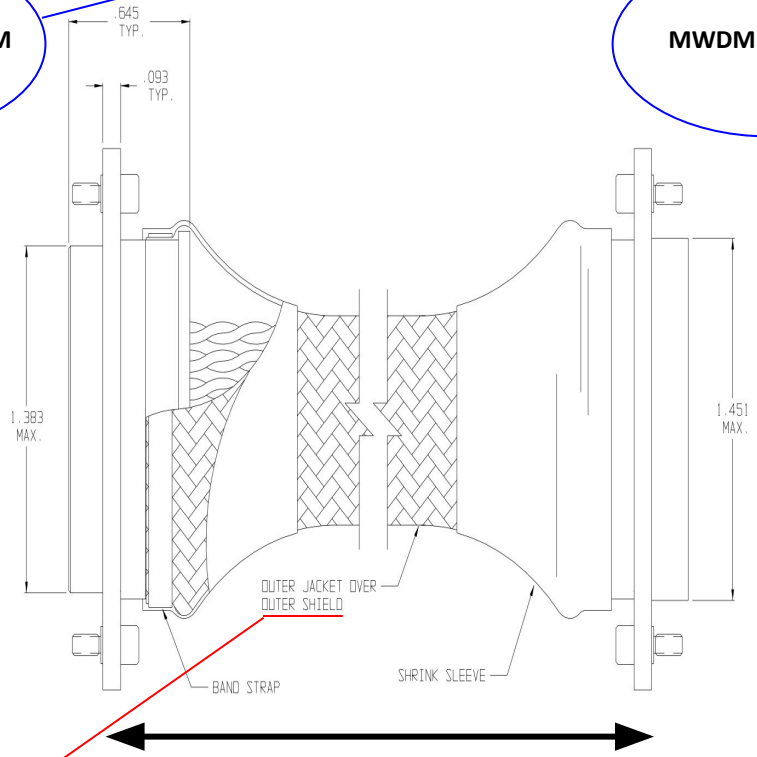
Glenair p/n (for cable assembly) : 1770-4740 - XX with XX the cable length in inches.

Temperature: 300K->300K

Cable schematic and pinout

Glenair p/n MWDM1L-100PSM

Glenair p/n MWDM1L-100SSM



XX = 750 mm -0/+50mm

Note: no individual pair shields (do this instead on back of MCE or 300K end manganin cable).

BUILD AND TEST IAW MIL-DTL-83513.

INTERFACE DIMENSIONS IAW MIL-DTL-83513.

MATERIAL/FINISH:
SHELL - ALUMINUM/CADMIUM
INSULATOR - LCP/N/A
CONTACTS - COPPER ALLOY/GOLD PLATED
WIRE -
  SINGLES - 30 AWG, M22759/33-9
  TWISTED PAIRS - M27500-30SC2U00 (30 AWG, M22759/33)
HARDWARE - M83513/05-12
BAND STRAP - STAINLESS STEEL
SHRINK SLEEVE - IAW M23053/5
OUTER SHIELD - COPPER/NICKEL, IAW GLENAIR 100-003
OUTER JACKET - HALAR, IAW GLENAIR 102-022

For more info on Glenair shielding options see here. Specifically here for shielding type 100-003 spec'd, and here and here for comparisons between it and other Glenair options (which are lighter but less effective).

300K->4K/1K 100-way manganin cables

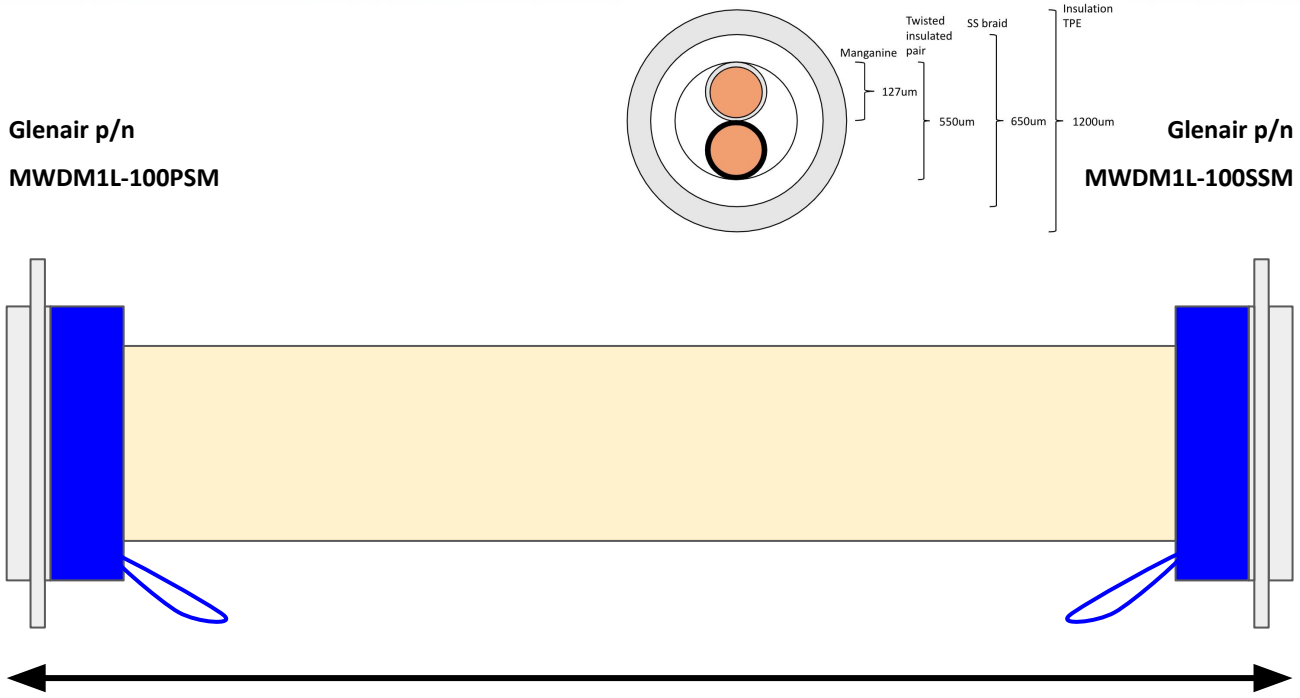
Manufacturer : Tekdata

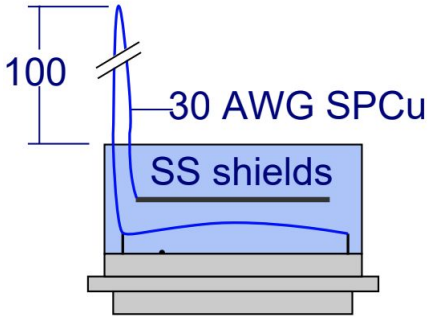
Temperature: 300K->4K/1K

No. of conductors: 100
Connectivity: direct pin to pin (i.e. 1-1, 2-2, …)

Pairing for cables:
Pair pins: 2-52, 3-53, … 25-75
Pair pins: 27-76, 28-77, …
51-100
Shield pins: 1 & 26

Loop shield connection out of potting on both ends to allow pins 1 & 26 to be disconnected from the shields by cutting loop (pins can remain connected to each other inside the potting). Sufficient loop length must be present to allow re-splicing if desired.





Construction:
2 x 25 pairs 36 AWG manganin with FPI dielectric
SS braid shield
FPI Jacket
Fibre is Nomex
Epoxy is Stycast 2850/09

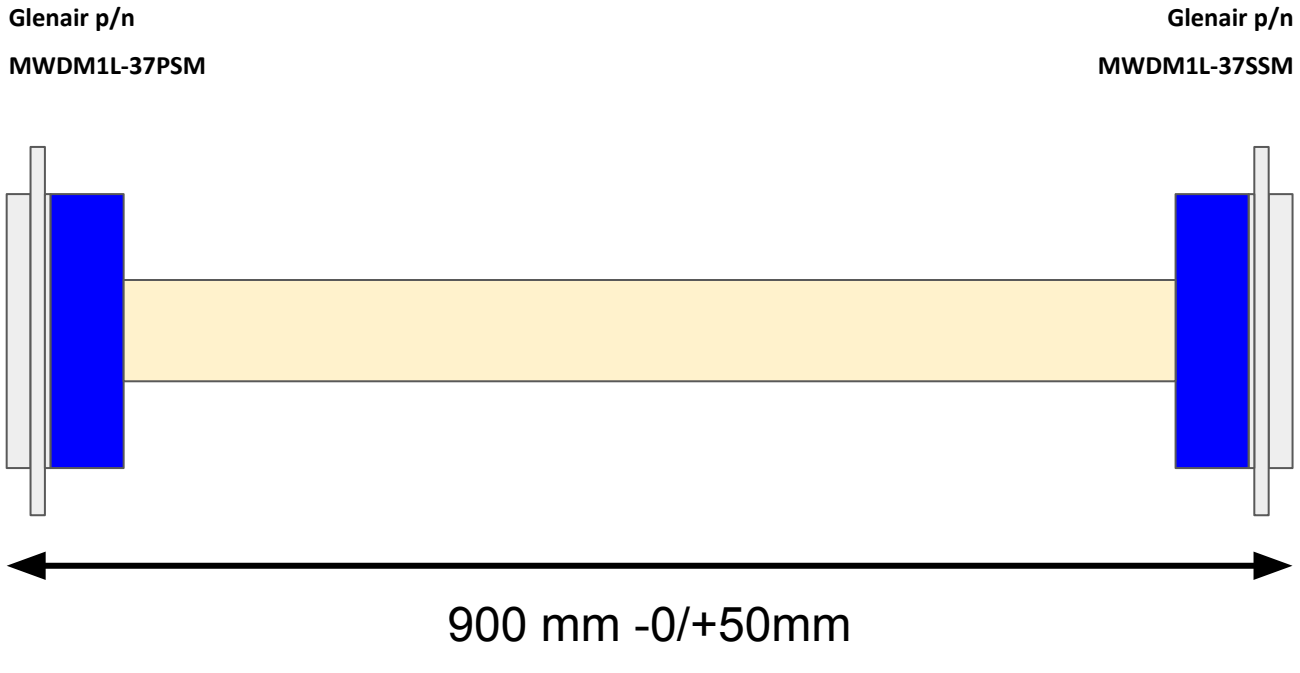
4K/1K → 100mK 37-way NbTi cables

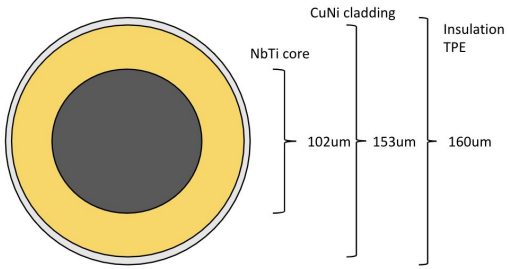
Manufacturer : Tekdata

Temperature: 4K/1K->100mK

No. of conductors: 37
Connectivity: direct pin to pin (i.e. 1-1, 2-2, …)

Pairing for cables:
Pair pins: 1-20, 2-21, 3-22, … , 18-37.
Shield pin: 19





Construction:
Conductors: 37 x 38 AWG NbTi CuNi clad twisted pairs in left and right hand alternate Lay and one single
Planar fibre: DuPont Nomex
Encapsulations: stycast 2850/09