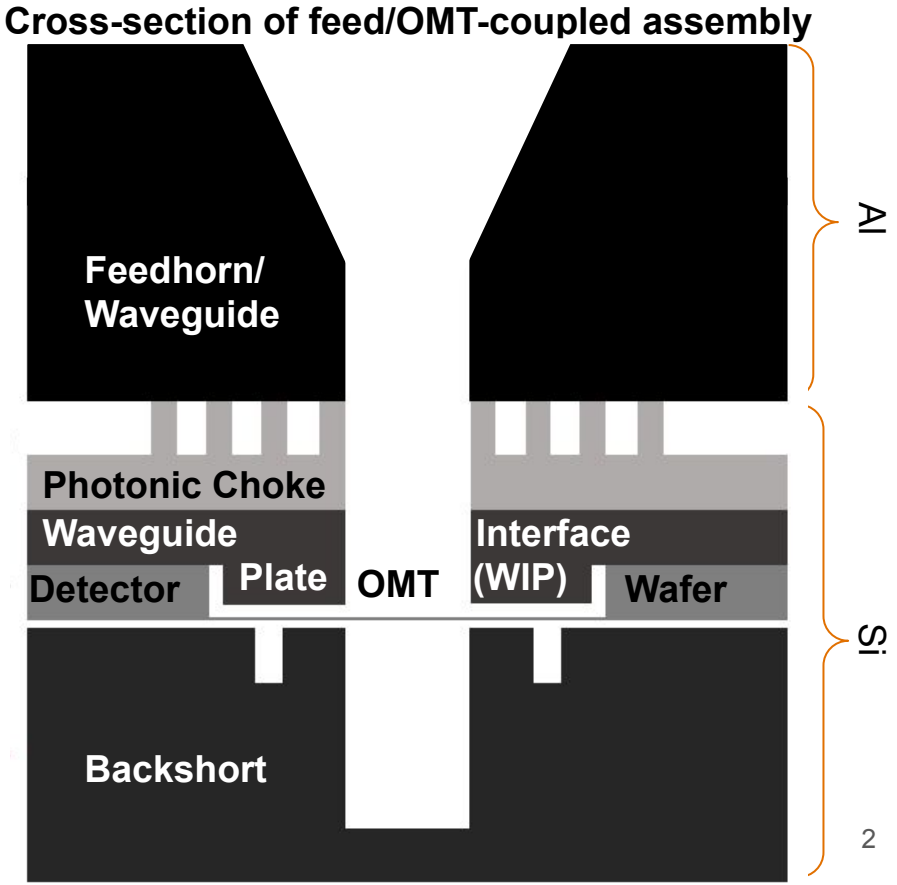
Optical Coupling

Sara M. Simon
03/11/21

CMB-S4

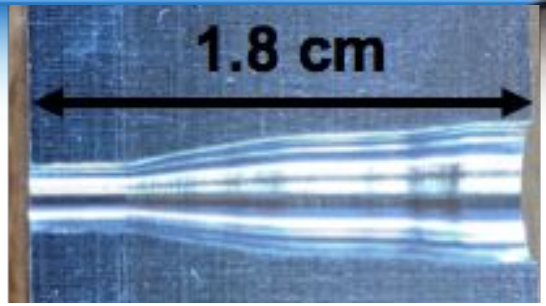
Baseline Plan Snapshot

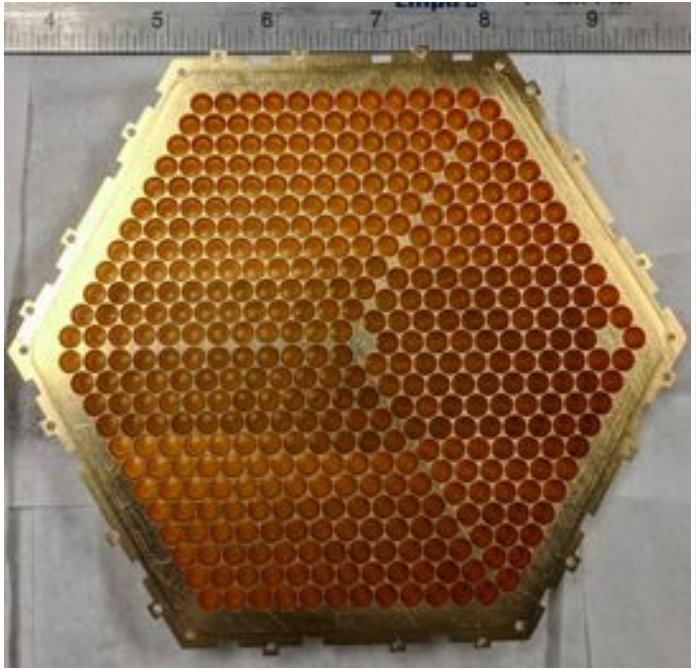
- Spline-profiled feedhorns coupled to OMT with coupling wafers
- Feedhorns are Al 6061
- Si coupling wafers include:
  - Photonic choke
  - Waveguide interface plate (WIP)
  - Backshort



Feedhorn Arrays

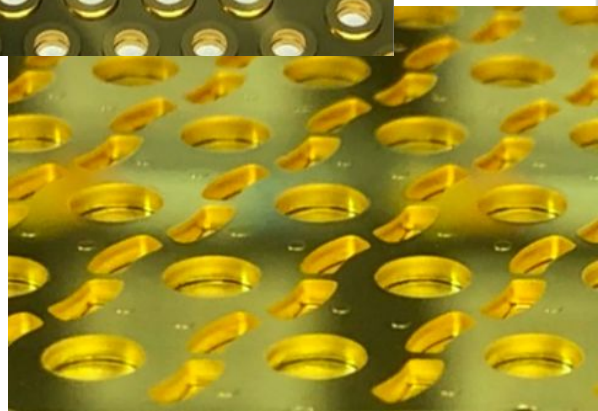
- Spline profiles optimized for performance requirements→ simulated estimates of systematic effects, efficiency
- Fabrication experience/testing from Simons Observatory
- Test arrays can use quick/less-optimized designs
- Final design requires set inputs:
  - Set pixel size
  - Defined waveguide cutoff and bands
  - Aperture stop angle
  - Any mechanical constraints (e.g. length)
  - Set input requirements
- Will need to decide when inputs are frozen





Interface Wafers

- Identifying commercial vendors
  - NIST made previously, handing off process
  - NIST could produce a few for early optical tests depending on available resources
- Process Overview:
  - Vendor 1: DRIE etch, inspection, and cleaning of the wafers→ RFI in progress
  - Vendor 2: TiCu seed layer (likely same vendor NIST uses)
  - Fermilab: Assemble WIP and choke into a single piece
  - Vendor 3: Cu/Au coating with gap filling (likely same vendor NIST uses)
  - Fermilab: Integration with detector wafer
- Process could be costly→ also considering alternatives to baseline



How much do different layouts with the same frequency bands complicate things?

- Different layouts with the same frequency bands
  - Different horn if the pixel sizes are different
  - Can use same interface wafer design and same SOI wafers, but need a different layout (including locations for backshort posts)
- Feedhorns
  - Each fully optimized and vetted horn design → ~1 month of time
  - Designs would have different lengths→ module design has to adjust
  - Reamers are pretty cheap ~$1-2k/ design
  - Programming layout for machining would be main cost ~20-40 hours programming time
- Interface Wafers (assuming space to use same design)
  - New layout
  - Different fab

How much do different frequency bands complicate things?

- Different frequency bands with the same layout
  - Different horn, OMT, and interface wafer designs because want to optimize OMT bandwidth to avoid losing a few percent in performance → Different waveguide cutoff, backshort, WIP, chokes
- Feedhorns
  - Each fully optimized and vetted horn design → ~1 month of time
  - Designs could have different lengths→ module design has to adjust
  - Reamers are pretty cheap ~$1-2k/ design
  - Less difficult to program machining (just change depth)
- Interface Wafers
  - Different layout and design
  - Design optimization ~few month timescale
  - Different SOI wafers
  - Different fab process
- Different layouts/frequency bands = New horn design and fab, new interface wafer fab (+ design and wafers for different frequency), new testing and verification of all components

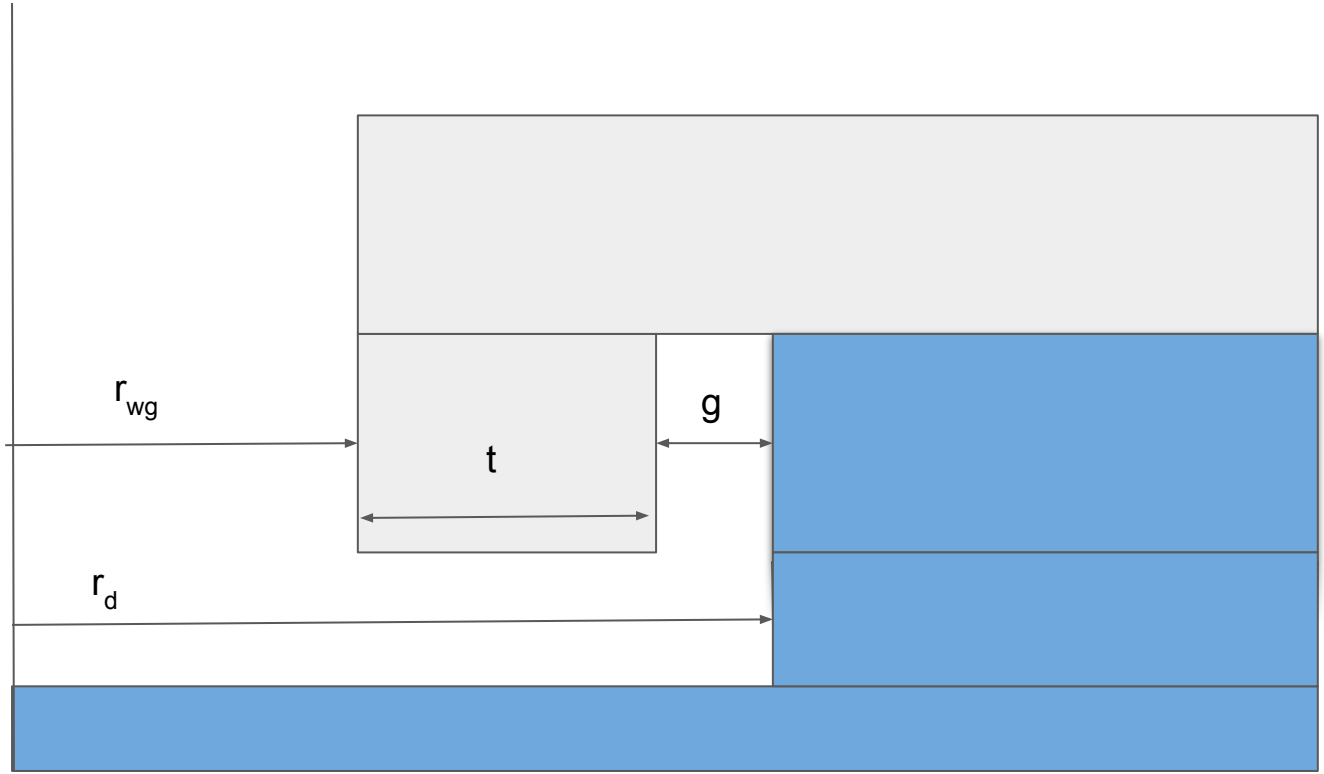
Alternatives to the current baseline

Other ideas to follow up on

- Design studies/demonstrations on simplifying the design
  - Do we need backshort moats? Do they need to be filled? (NIST interested)
  - Exploring ways to decrease the gap in the waveguide as a means to lessen dark pickup (NIST interested)
  - How much do we need the photonic choke? (Likely more wiggle room at LF)
- Fabrication simplifications:
  - Could we use Si machining for LF/ULF? Look into Cold Quanta
  - Can we use alternative materials? (more on this)

Can we make the coupling wafers with other materials?

Differences in coefficient of thermal contraction (CTE) of WIP with detector would be the first concern



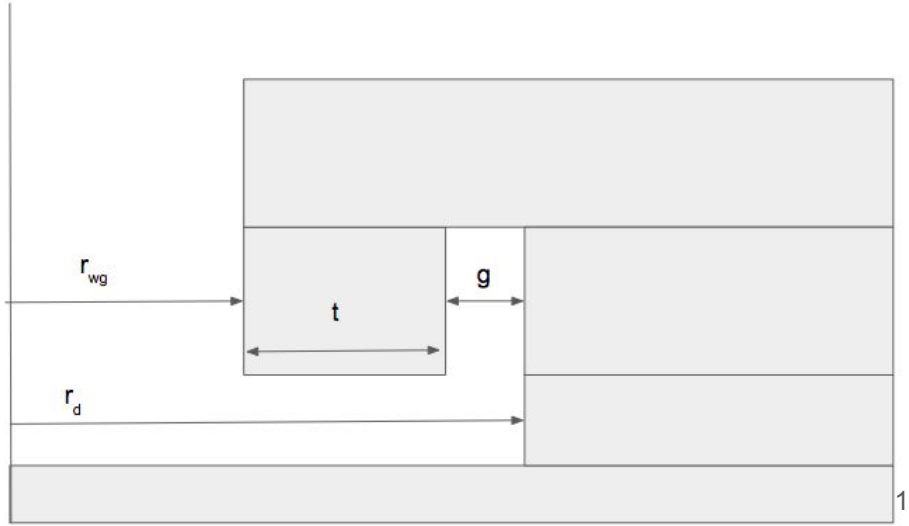
Naive Scalings

- r_{wg} and r_d scale with frequency (roughly)
- g stays the same with frequency (roughly)

$r_d - r_{wg} = g + t$

(g+t)=750 um* 75 GHz/(lower band edge freq)

	g+t	t (g=25 um)
ULF	3214 um	3189 um
LF	2344 um	2319 um
MF	750 um	725 um
HF	288 um	263 um



Rough displacement of WIP at farthest pixel

L=65 mm (~ farthest pixel)

Note: Invar very close to Si, but difficult to machine and magnetic properties are worrisome→ Is this enough to eliminate it from consideration?

Material	$\Delta L/L$ ($x10^{-4}$)	ΔL (um)
Al	41.4	269
Mo	10.6	69
CE7F	9	59
AlMoSi	(very close to Al, slightly less)	

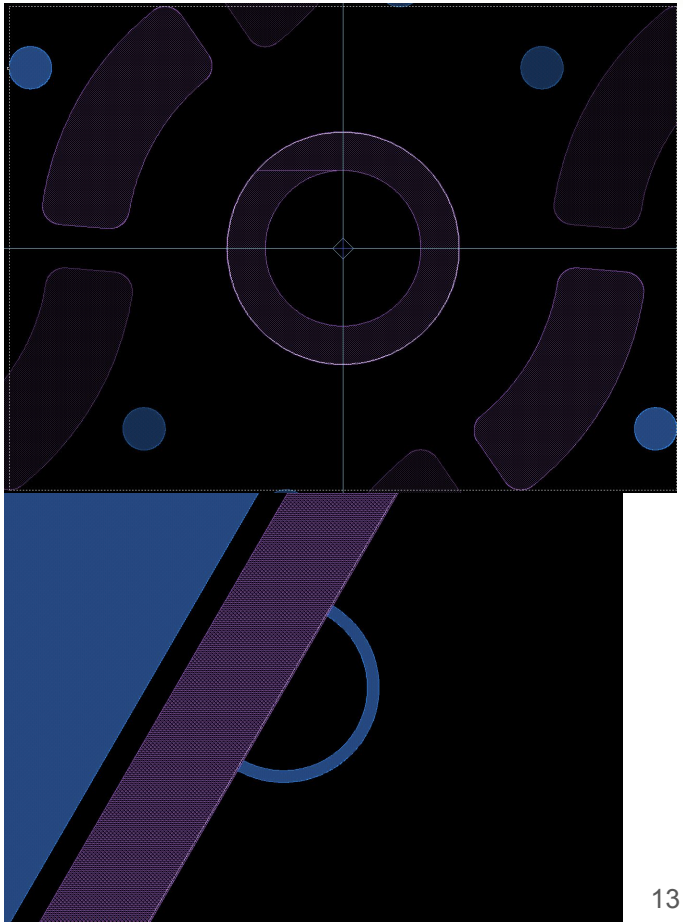
Adjusting the gap size

- Need ≥25 um gap size cold (in most central pixels CTE shift will be small)
  - Total g = 25 um + ΔL
  - Assume <500 um annulus is marginal for machining
- Al 6061/AlMoSi: Impossible for HF, marginal for MF, LF/ULF okay
  - 3D printed AlMoSi likely rougher surface + lower tolerances than Al6061, non isotropic CTE
- Mo: Marginal for HF, MF/LF/ULF okay
  - Very difficult to machine, 3D printing in very rough early phase→ likely not feasible right now
- CE7F: Marginal for HF, MF/LF/ULF okay
  - MF tolerances difficult to hit + may be cost prohibitive, LF might be feasible

- Al6061 and CE7F could be feasible options for LF/ULF arrays

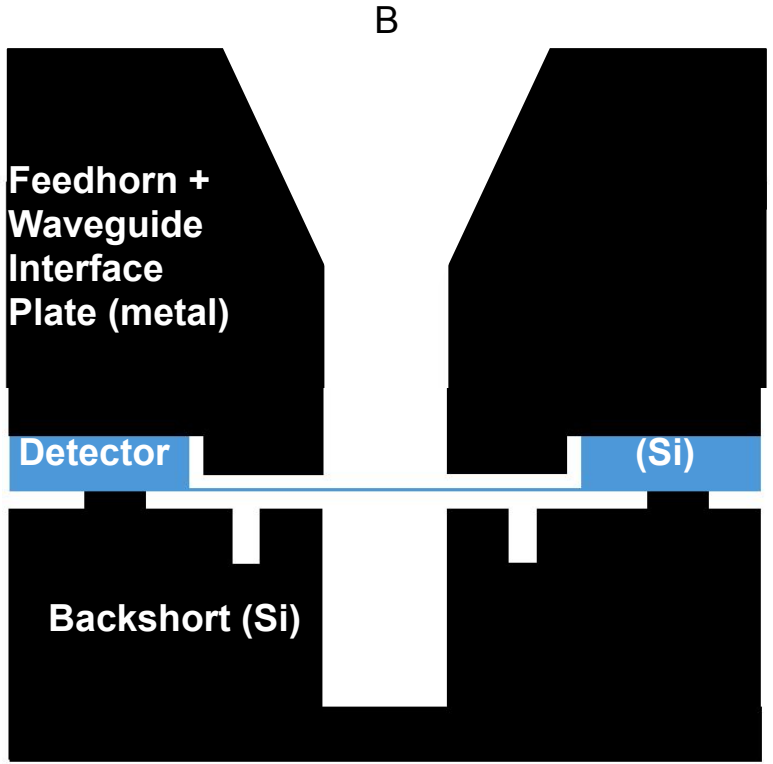
Current backshort design needs to be CTE matched

- Backshort has two key features
  - 10-20 um tall posts that make contact with the detector array
  - 10-20 um tall fences around glue divots
- If post location changes with cooling, it will scrape against the RF circuitry and wiring on pixels
- Glue fences are close to the wiring and bonding pads
- Would need a redesign of how backshort couples to array to feasibly make it from another material



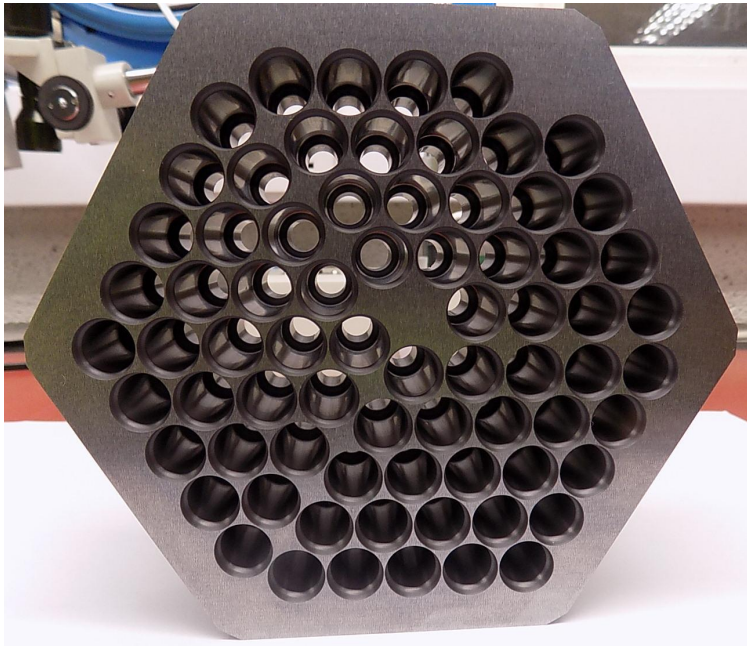
ULF/LF Horn+WIP Concept

- Might be feasible to nix the photonic choke and have the feedhorn piece include the WIP boss for LF/ULF
  - Flatness below boss feature will be the primary difficulty
  - Photonic choke not as critical at LF because gap sizes are smaller compared to wavelength→ will need to check with modeling



CE7F

- Proprietary machining (machines like ceramic), tapped holes need helicoils
- Sandvik made the 27/39 GHz feedhorns for AdvACT
  - Have their own Au-plater
- Made an interface plate for CLASS that has a similar feature to WIP boss→ wire EDM
- Throughput seems feasible
- Sandvik technicians think LF pieces would be feasible→ would need to do some tests to see what tool wear and tolerances for WIP boss look like
- Might be worth investigating depending on cost of Si interface wafers (or Al feasibility)



Other Items for discussion?