

Module Design and Assembly

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CMB-S4 Collaboration Meeting
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High-Level Overview

- Early design work identified several areas requiring additional R&D in order to satisfy existing system interface requirements (e.g. requirement of superconducting flex cables, module pitch in SATs)
- Does not make sense for early (“CDFG”) detector testing to depend on outcomes of R&D for production modules
- To enable early integrated tests of CDFG detectors + some readout, we are forking the module design:
 - **“CDFG module”** - Simple design using shovel-ready hardware that fits in the cryostats identified for CDFG testing (FNAL, Illinois, SLAC)
 - **Production module** - Module that we will actually deploy, satisfying all project interface requirements

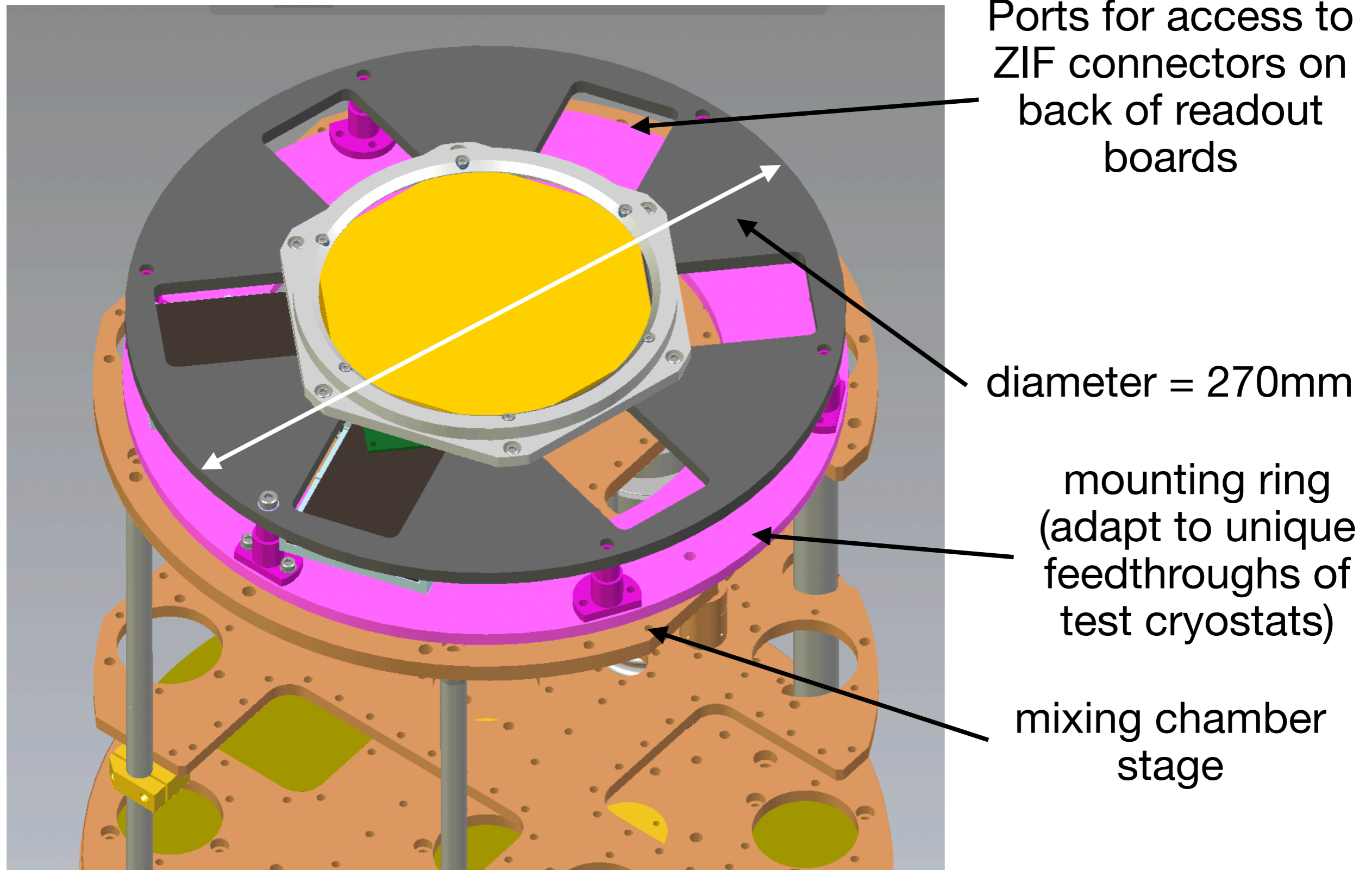
Module R&D Areas

- *Superconducting flex cables are required by readout/module interface*
 - Limit of conventional flex PCB fab (e.g. TechEtch) is around ~9mils pitch; need 4mils pitch; other processes have higher resolution, but higher cost and limited vendors
- *SAT module pitch of 124mm*
 - Forces flex cables on top of backshort with step bond, which complicates mounting and requires wire bonding R&D
 - Limits mechanical space in ways that require some study: less room for magnetic shielding (low-f noise risk) and focal-plane mounting structure (vibrational risk)
- *Readout density and assembly*
 - Packaging readout for SAT HF (1876 detectors) requires significant area of readout electronics
 - Challenging to fit these behind the detector wafer footprint in a way that can be bonded and assembled without elaborate origami

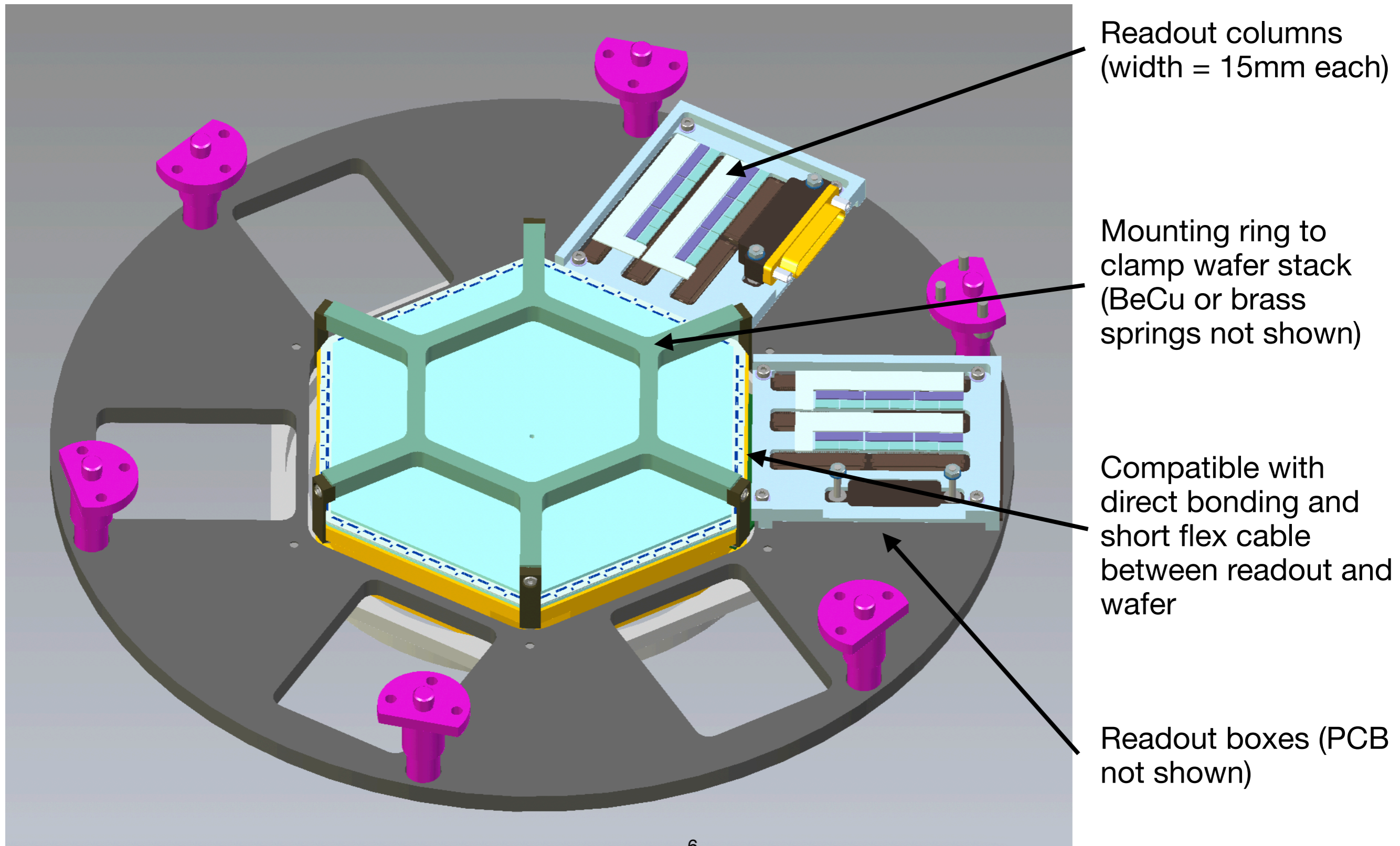
CDFG Testing Module

- See specifications document
- Planar layout a la AdvACT to relax constraint on flex cable
- Use only 2 columns of readout per side of wafer to enable compatibility between SAT and LAT wafer pinouts
- Diameter of footprint needs to be $<290\text{mm}$ to ensure compatibility with initial three testbeds (FNAL, Illinois, SLAC)
- Exploring use of SO-style horn arrays fabricated at Michigan (SO shop) to expedite acquisition
- Keep connectors and wiring of readout as similar to deployment module as possible (MicroD 37-pin for bias lines, ZIF for row select, etc.)

Mounting in LD400 Cryostat



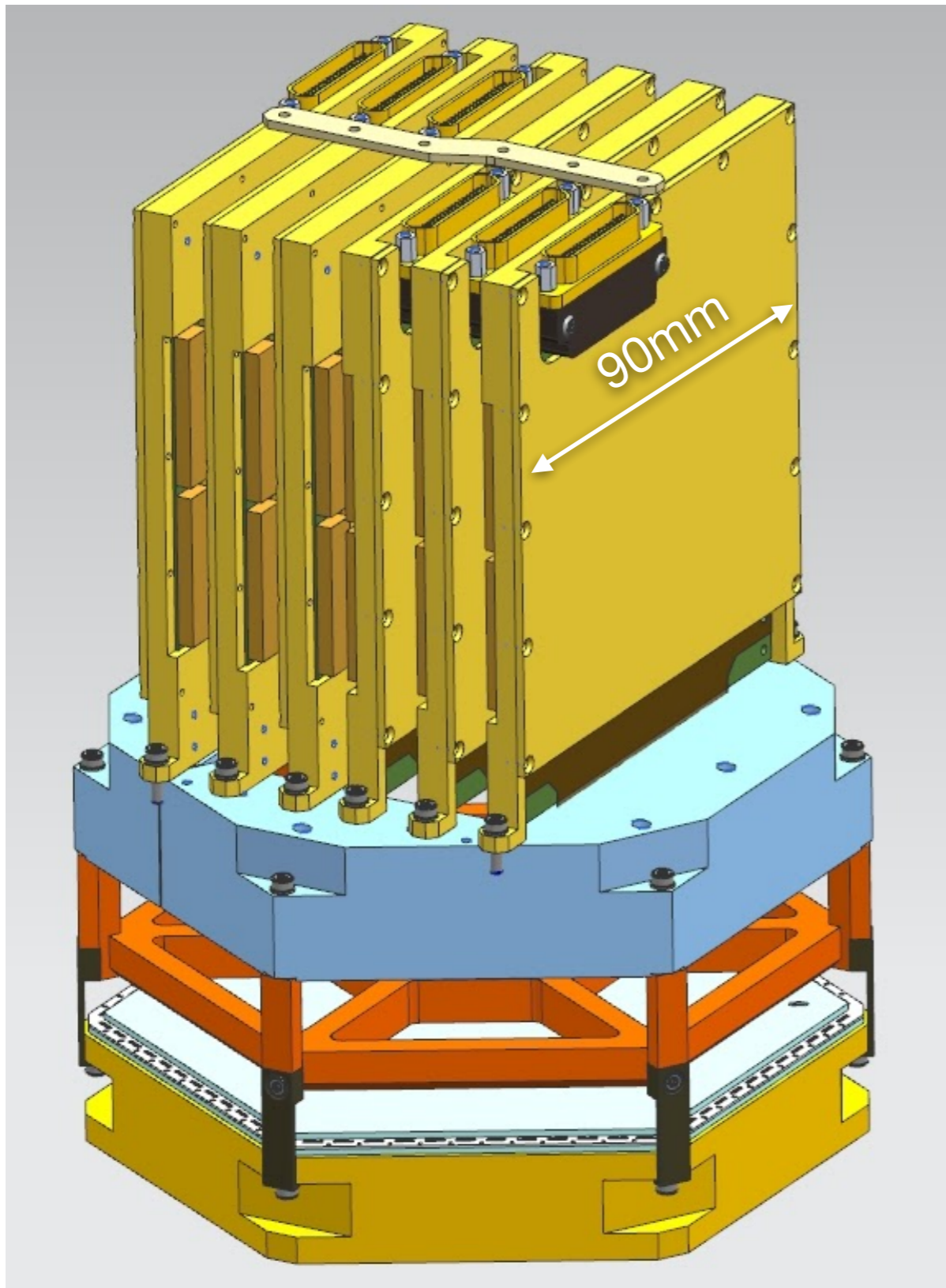
Back View



CDFG Module Next Steps

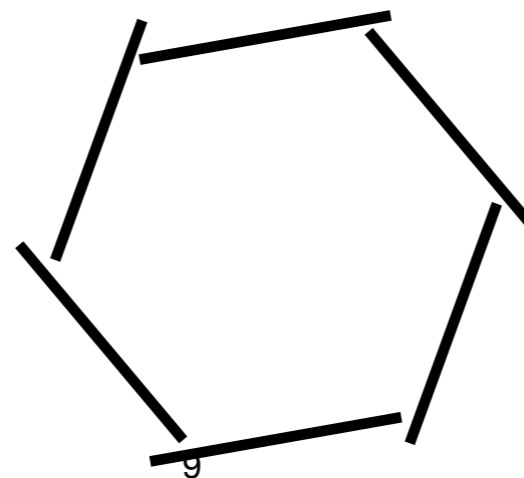
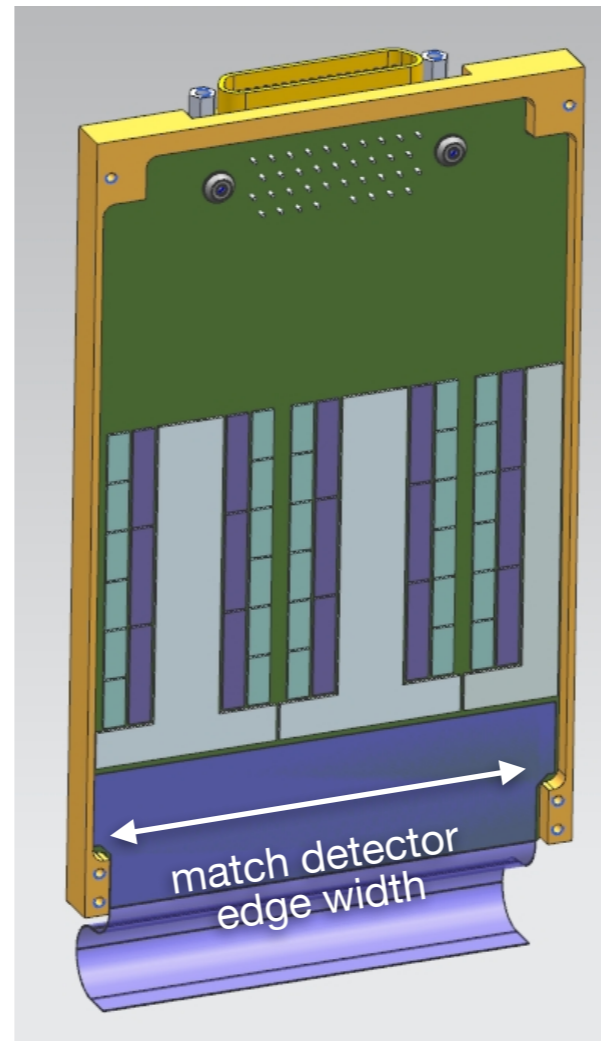
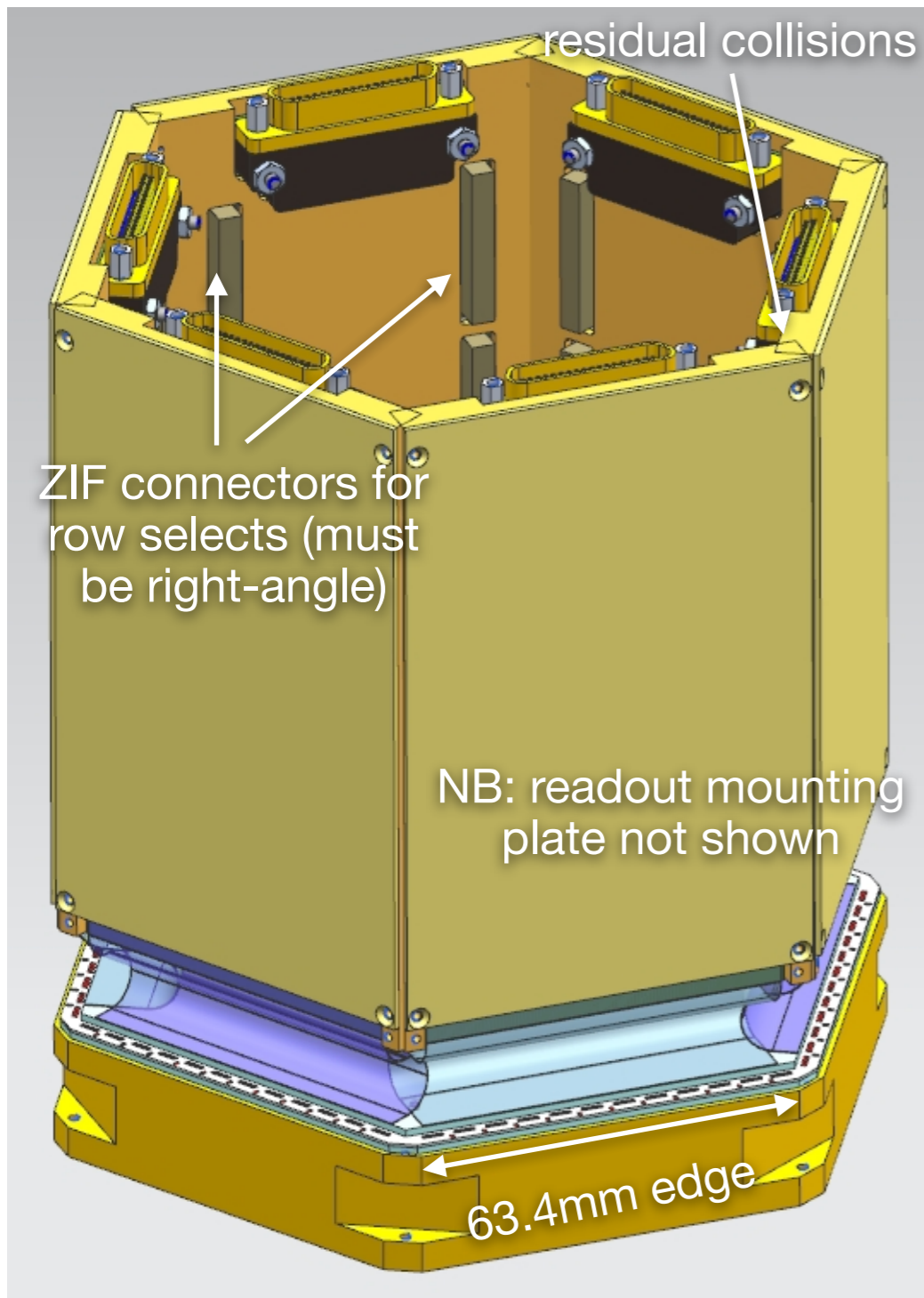
- Final iteration on readout box design with readout working group (G. Haller, Z. Ahmed)
- Quantify minimum magnetic shielding needed for TDM readout in test cryostat configuration
- Simple simulations of magnetic field suppression in SLAC, Illinois, FNAL test cryostats to verify that we meet shielding spec
- Tweak mounting to avoid collisions with wiring feedthroughs, other fixtures, in test cryostats

Production Module - v1



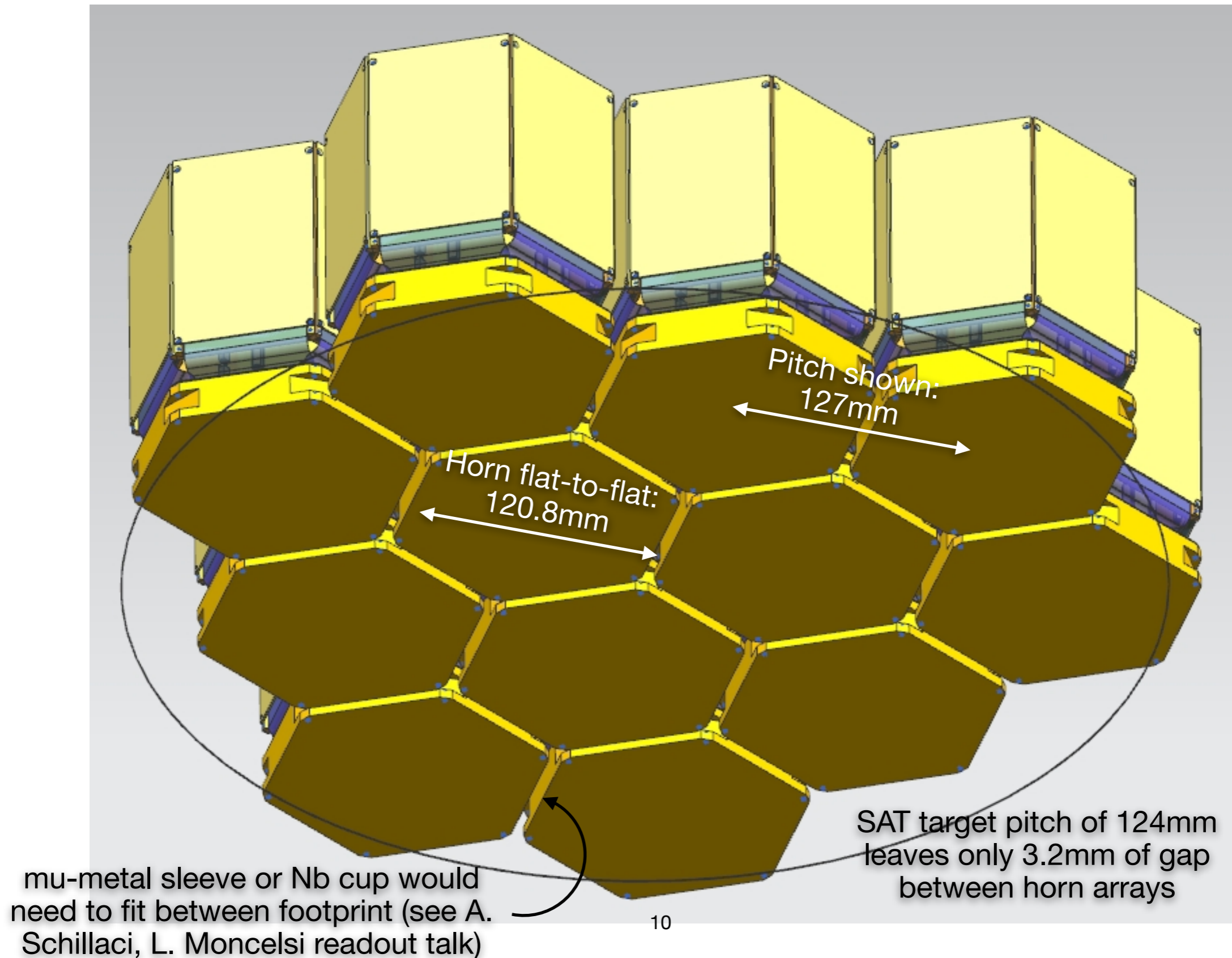
- First module concept that met key interface requirements
- 90-mm width readout boxes on back, barely fit behind wafer footprint
- Flex cable (not shown) requires complicated routing from edge of wafer to box, with 60deg bend
- Long cables are difficult to assemble and fabricate, put pressure on inductance budget

Readout Boxes - v2 in progress



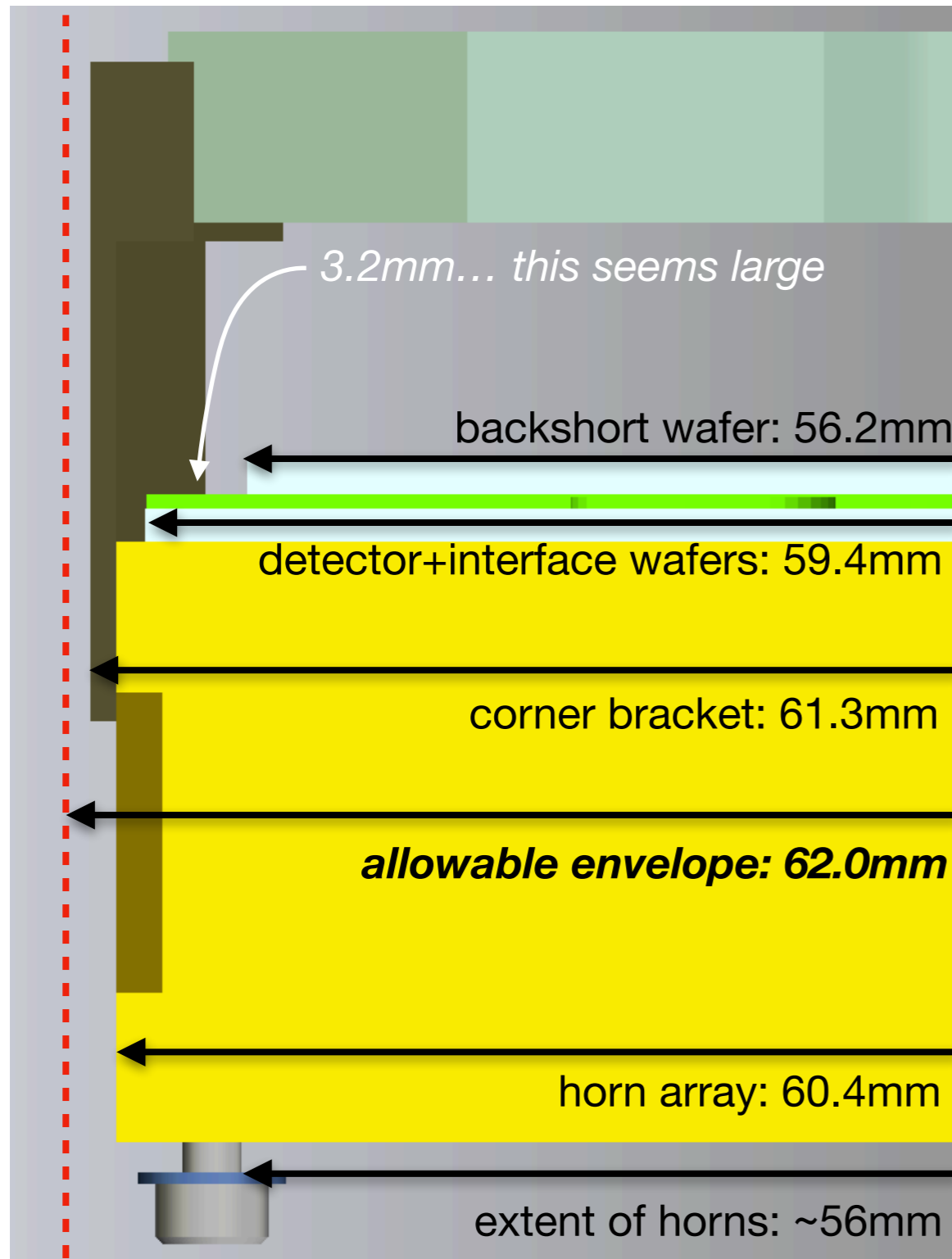
- Achieved significant reduction in box width with denser wiring chips, corrected MUX chip dimensions (90mm -> 65mm)
- Flex cables drastically shortened, eliminated twisting/routing problem
- Final layout/dimensions of readout box pending final MUX column wiring chip configuration (see G. Haller readout talk)
- Residual collisions in corners, resolve with some combination of fine-tuning box width, removing material, and “pinwheel” orientation
- Include springs on readout mounting plate as on previous slide

SAT Focal Plane Configuration



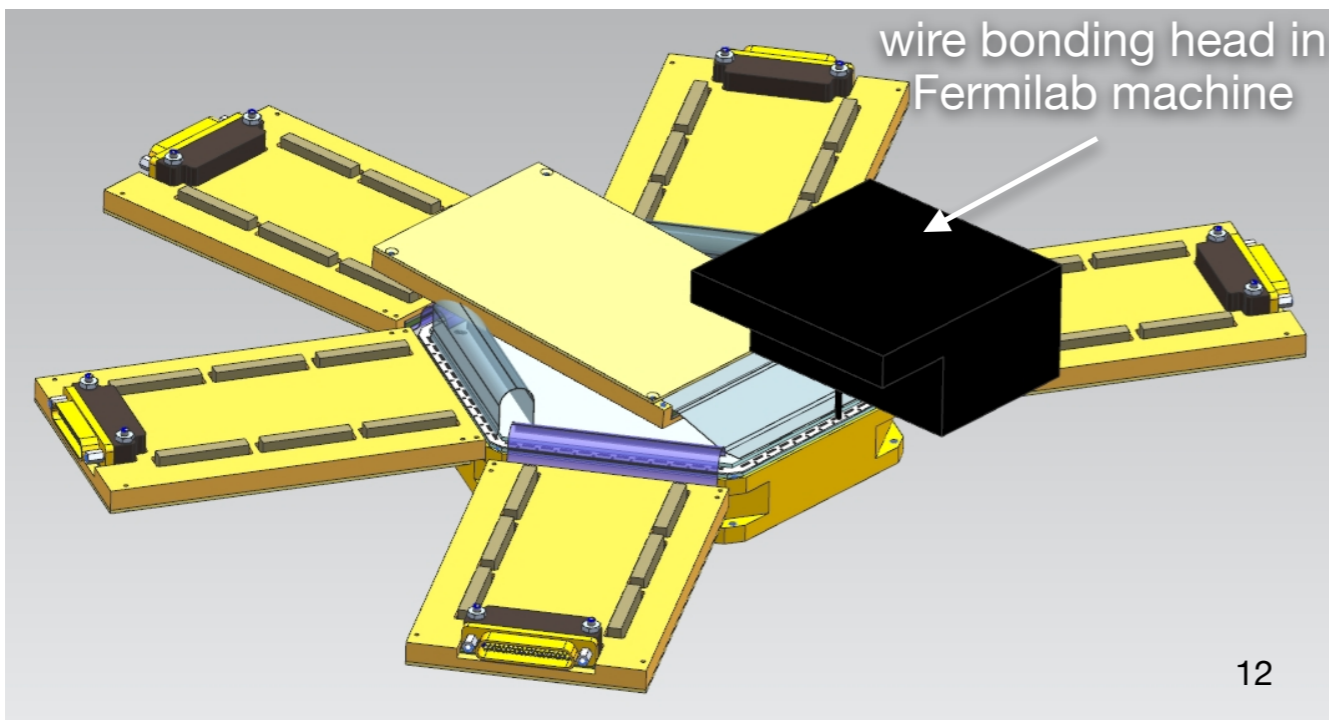
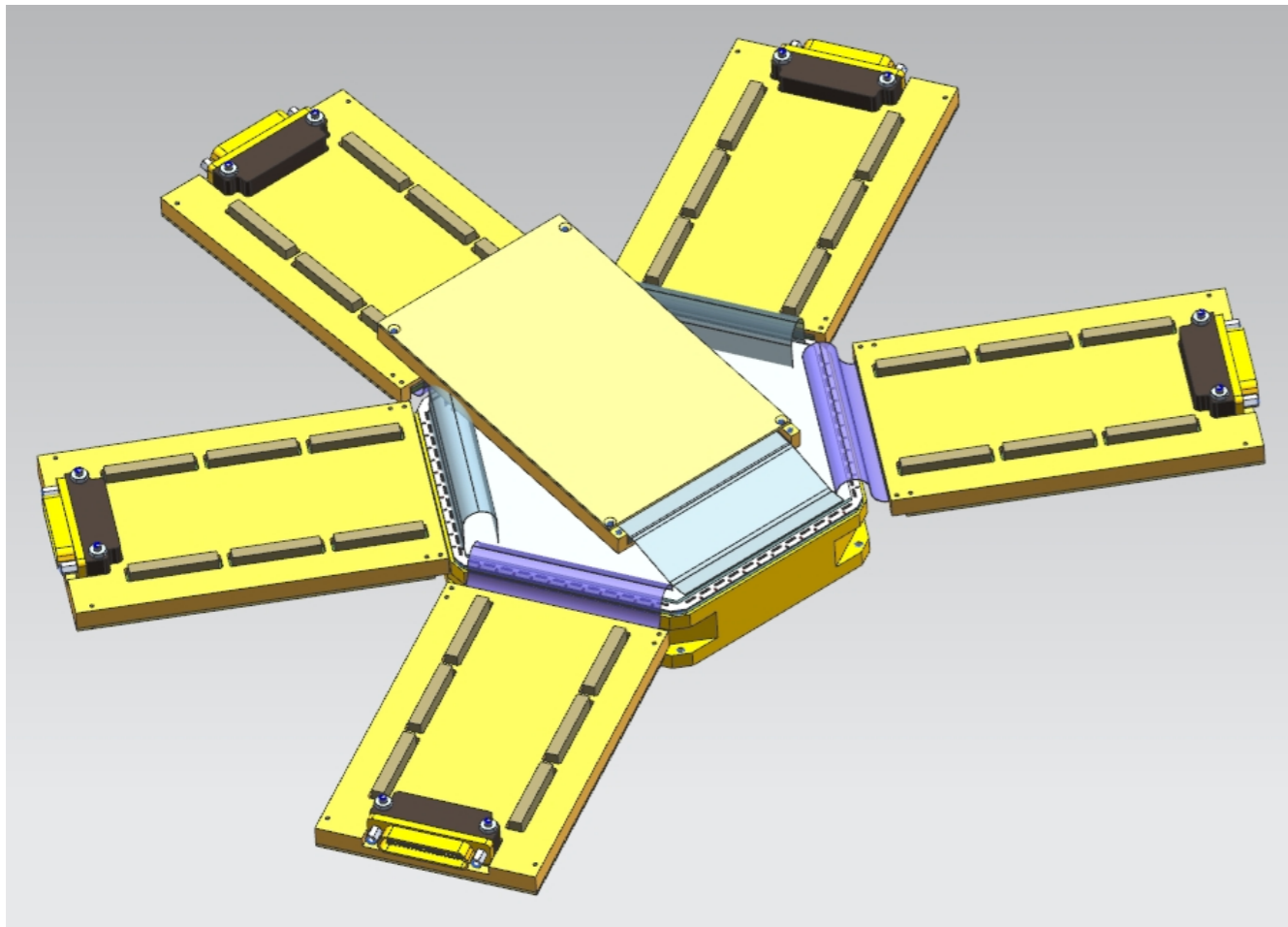
SAT Pitch Problem

Important radial distances:



- In current design, there is 1.6mm or 0.7mm clearance for focal plane plate + magnetic shield, modulo precise locations. Seems inadequate.
- Possible solutions:
 - Relax 124mm pitch: reduces SAT mapping speed.
 - Shrink detector+interface wafers and horn array, holding backshort and horn array by ~2mm. *No impact to optics*. Reduces area for bondpads and mechanical support of outer horn wall.
 - Eliminate focal plane plate, and expand horn arrays to bolt directly into each other. Probably too radical, but arguably not insane.

Assembly



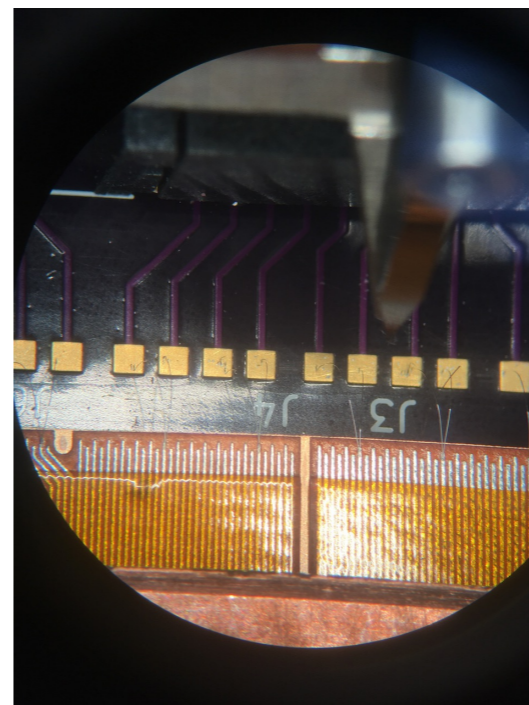
- Because of SAT pitch requirement, flex cables must mount inward (detector wafer is 119mm and pitch is 124mm)
- In order to maintain bondpads on same side of flex cable at both ends, box must fold back into backshort during bonding
- Jig needed to hold boxes during bonding steps
- Head of Fermilab wire bonding machine is non-trivial in size—critical to include in 3D model of assembly

Flex Cables

- Superconducting flex cables are key R&D problem; no extant solution meets volume, cost, and trace density requirements
- Considered two options:
 1. Superconducting aluminum, 2mils/2mils trace/space (1-layer) or 4mils/4mils trace/space (2-layer)
 2. Tinned copper, 2mils/2mils
- Explored 15 vendors, remaining options include:
 - SLAC has process that can make 90um pitch Al traces on polyimide substrate; could commercialize
 - Try to tune tin layer on copper substrate to achieve lower R_p

Vendor / heritage	Stack	pitch (trace/space)	R (T=100mK)	Ic	Cost
TechEtch / SPT-3G	polyimide / 9um tinned Cu / polyimide	2mils / 2mils	7-10 mOhm (~4 inches) (expect 50mOhm for RRR~100)	No SC transition observed	~\$250
TechEtch / PB2a	polyimide / 50-300uinch tinned Cu / polyimide	2mils / 2mils	Cooling down	Cooling down	~\$250
TechEtch / SPIDER	polyimide / aluminum / polyimide	4.5mils / 4.5mils	Bonded, in queue	Bonded, in queue	~\$250
Flexible Circuits Technology	polyimide / 1 mil Al / polyimide	4mils / 4mils	fab failed	fab failed	~\$250
SLAC	polyimide / Al	90um	TBD	TBD	TBD

TechEtch claims yield drops significantly at <9mils pitch in Al



TechEtch / SPIDER



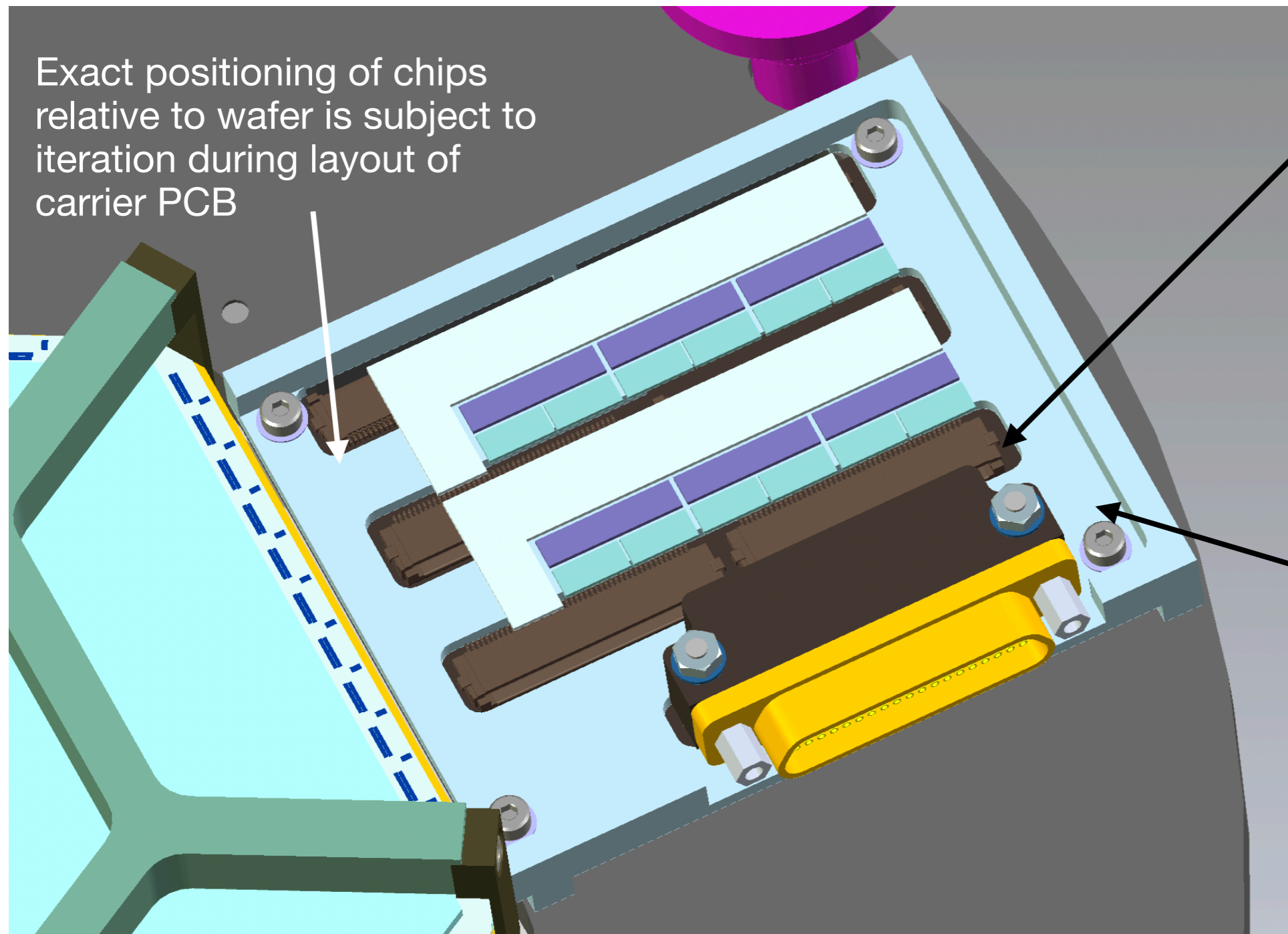
SLAC (90um Al)

Next Steps

- CDFG test module is straightforward and will proceed in tandem with readout layout
- Production module with readout boxes parallel to each side of hex (v2) is probably viable
- Need to finalize readout box mechanical design together with readout layout
- Flex cables remain a major R&D task
- Further study and implementation of magnetic shielding

Backup

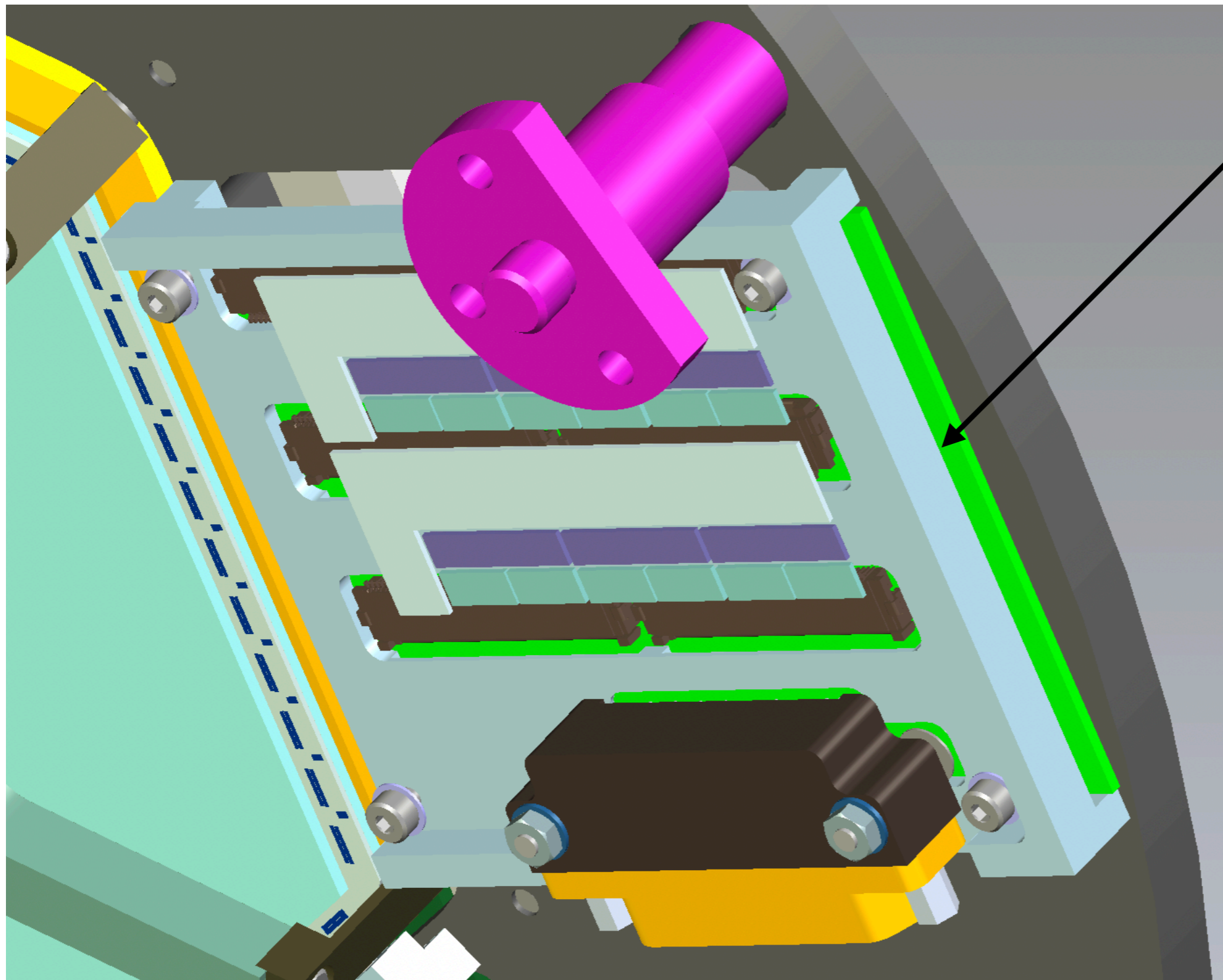
Readout Box Detail



6x 45-position ZIF connectors on backside of PCB

Constrained PCB footprint doesn't allow much space for magnetic shielding of the carrier... needs to spec allowable B-field for lab testing

Magnetic Shielding Considerations



Accommodation for sheet of mu-metal for magnetic shielding; annular ring also possible

Level of detail in magnetic shielding strategy for readout in CDFG test module is extremely primitive. Further development and basic simulations needed.

Production Module - Key Interfaces and Requirements

- ***Readout:***

- MUX chips should be housed in modular boxes, necessitating use of superconducting flex cables
- Need to control inductance in superconducting wiring to TES (needs spec)

- ***Detectors:***

- 118.8mm wafer size (hex side-to-side); inherited from SO

- ***SAT:***

- 124mm wafer pitch (hex side-to-side); allows 2.6mm between edge of silicon and boundary of hex footprint
- Accommodations for mounting in a curved focal plane (*new this week*)

- ***Modules and assembly:***

- Assembly and wire bonding must be physically possible
- High-yield assembly must take 1 technician-day

Module design is highly sensitive to interface mechanical dimensions. Changes of ~1mm can make or break design configurations.