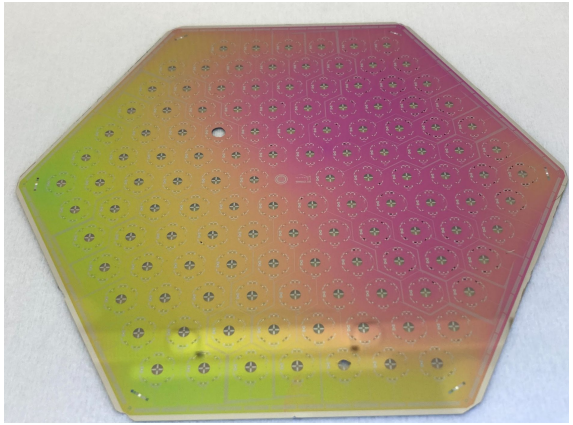
UCB CDFG Plan
CMB-S4 Detector Layout Workshop #2



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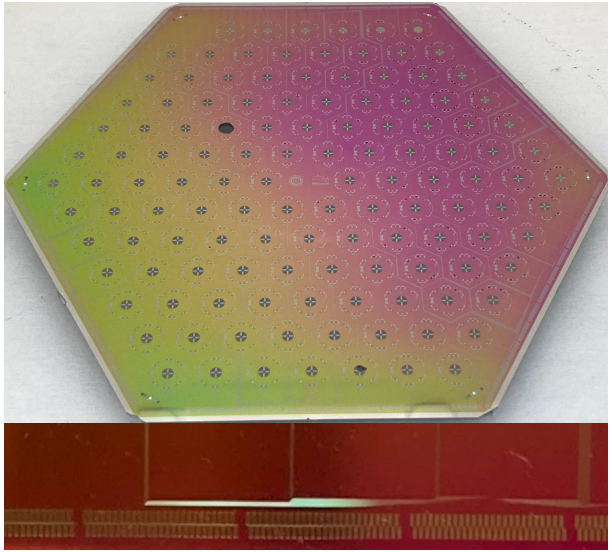
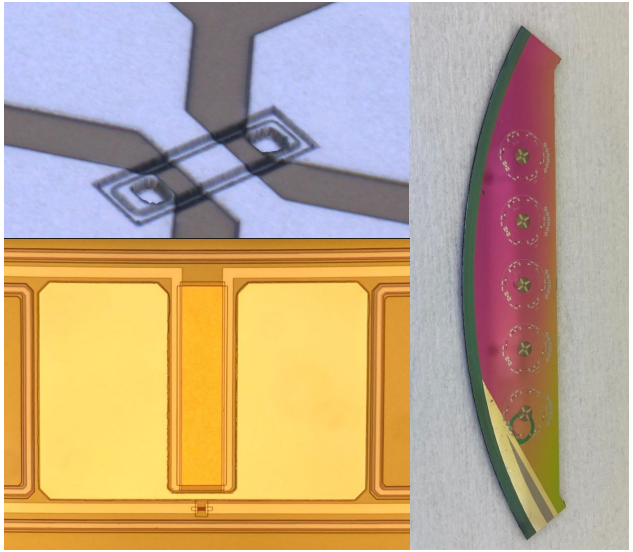
Prototype CDFG wafer

Process



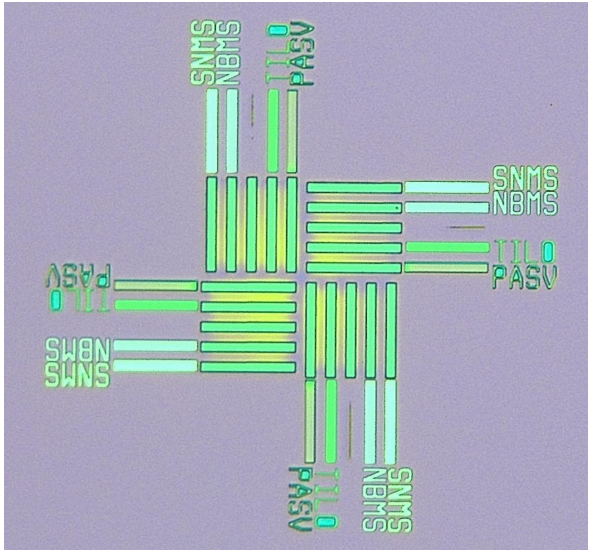
- Completed first CDFG wafer
- DRIE @ SeeQC
- Stealth Dicing @ GDSI
- Over >90% mechanical yield on released and diced wafer

Inspection



- Cross unders used for RF
- Witness pixels stay at UCB
- TES Island → Rn ~10mOhm
- First checks of performance happening now

Litho/Layout



- Interlayer alignment with MLA
- 45-50 mins per layer/wafer
- Compatible with UCB fab flow
- Compatible with rhombus+hex

Next CDFG steps

1. Receiving initial funding from CMB-S4
   - Dual TES (prototyped fabricated)
   - LF pixel R&D
2. Characterize first CDFG witness pixels
3. Development CMB-S4 bolometers
4. Improve robustness and yield of fab process
5. Improve in-house and intra-fab characterization for improve reporting